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SLC M/B Schematics Document

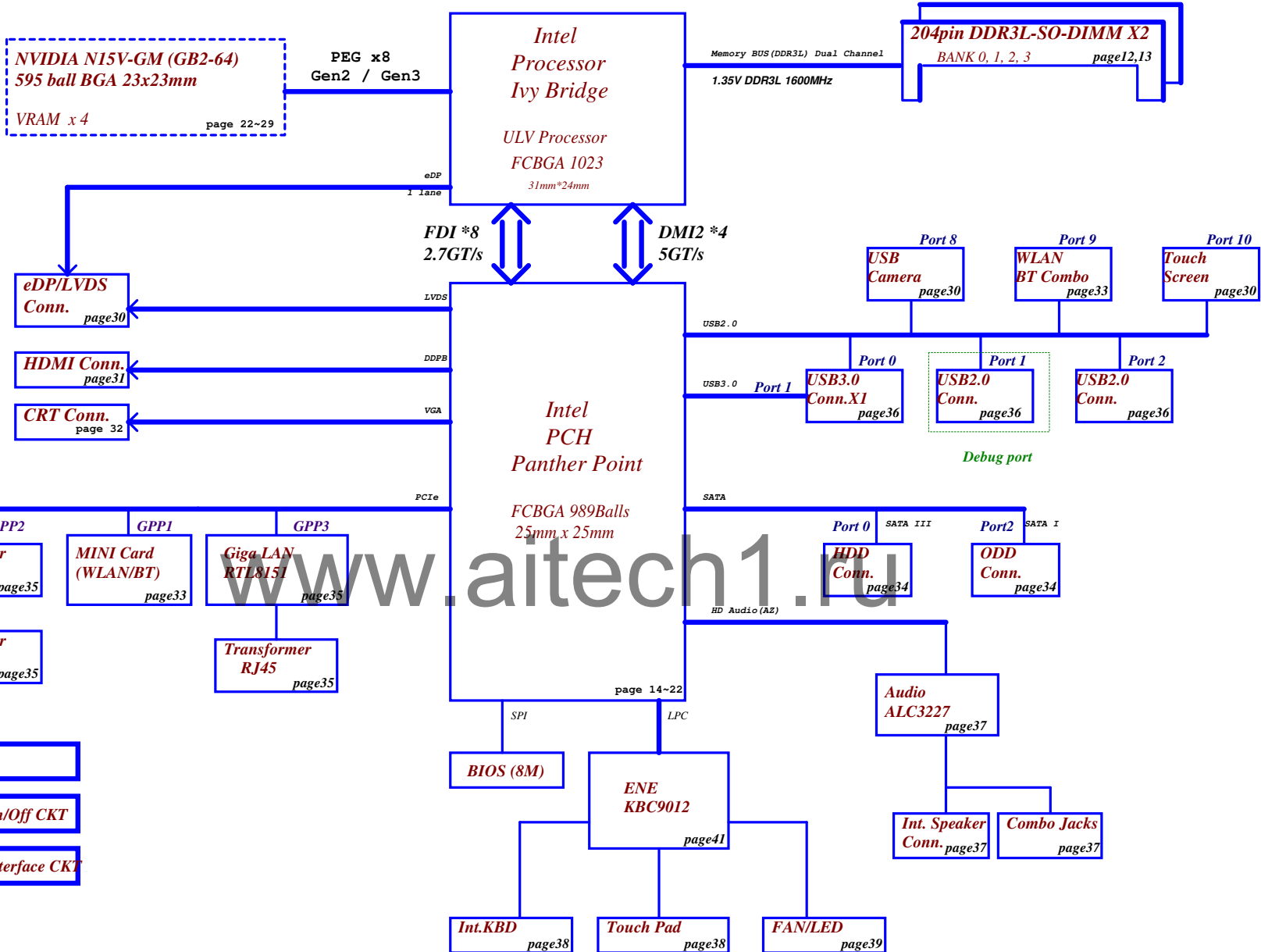
14" : Tabo; 15.6" Pochacco

Intel Ivy Bridge ULV Processor with DDRIII + Panther Point

Date : 2014/02/17

Version 0.5

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ZSO40/50 (LA-A998P/LA-A999 Ver:0.1)

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
		ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.675VS	+0.675VP to +0.675VS switched power rail for DDR3L terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.35V	+1.35V_VDDQP to +1.35V power rail for DDR3L	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+3VALW) to 1.8V LDO power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VL to KBC	ON	ON	ON*
+LAN_VDD_3V3	+3VALW to +LAN_VDD_3V3 power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Power Plane	Description	S1	S3	S5
+3VGS	GPU power	PX	OFF	OFF
+VGA_CORE	GPU power	PX	OFF	OFF
+1.05VGS	GPU power	PX	OFF	OFF
+1.5VGS	GPU power	PX	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	
G-sensor	0x50/0x52
Charger IC BQ24738	0xFFH

EC SM Bus2 address

Device	Address
PCH SML1	
N15V-GE dGPU	

PCH SM Bus address

Device	Address
DDR DIMM0	
DDR DIMM1	

SMBUS Control Table

	SOURCE	BATT	WLAN MIIN1	BATT Charger	TP	SODIMM	EC_SMB_CLK2 EC_SMB_DATA2	PCH_SML1_CLK PCH_SML1_DATA	G-Sensor	dGPU
EC_SMB_CLK1 EC_SMB_DATA1	KB9012	V		V					V	
EC_SMB_CLK2 EC_SMB_DATA2	KB9012							V		V
PCH_SMB_CLK PCH_SMB_DATA	PCH					V				
PCH_SML0_CLK PCH_SML0_DATA	PCH									
PCH_SML1_CLK PCH_SML1_DATA	PCH						V			

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	mini WLAN	CLKOUTFLEX0	None
			CLKOUTFLEX1	None
	CLKOUT_PCIE1	CARD READER	CLKOUTFLEX2	None
	CLKOUT_PCIE2	PCIE LAN	CLKOUTFLEX3	DGPU_PRSENT#
	CLKOUT_PCIE3	None		
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :
: means Digital Ground
: means Analog Ground

Project ID	UMA@	DIS@		
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PCB	LA-A998P	LA-A999P
	14@	15@

BY SKU		
TPM	9635@	9656@
CPU	CPUUMA1@ CPUUMA2@ CPUDIS@	
VRAM	X76@ MIC@	SAM@ HY@

Option	@	CONN@	SP@	PX@	UMA@	DIS@	
UMA	X	X	V	X	V	X	
DIS	X	X	V	V	X	V	

CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC/TPM
PCI2	None
PCI3	None
PCI4	None

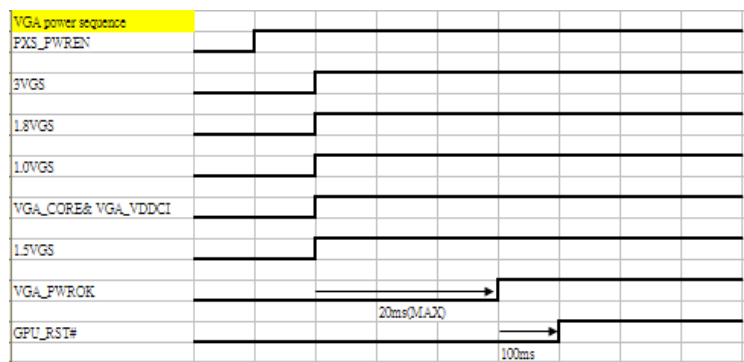
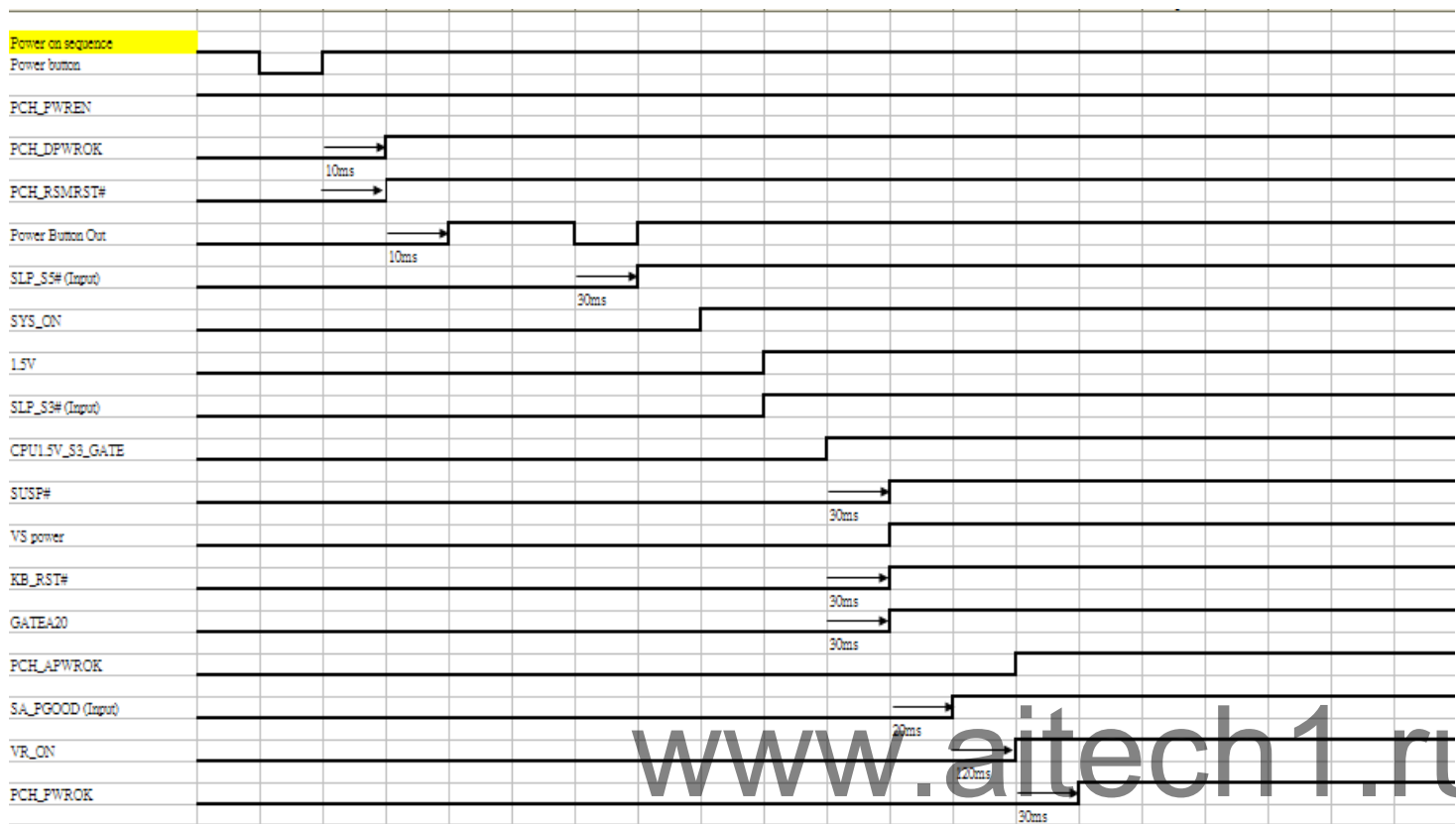
SATA	DESTINATION
SATA0	JHDD1
SATA1	None
SATA2	JODD1
SATA3	None
SATA4	None
SATA5	None

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB2.0 (For USB3.0 Conn.)
		1	USB2.0 (D/B)
		2	USB2.0 (D/B)
	UHCI1	3	None
		4	None
		5	None
EHCI2	UHCI2	6	None
		7	None
		8	Camera
	UHCI3	9	Mini Card(WLAN& BT)
		10	Touch Screen
		11	None
	UHCI5	12	None
		13	None

USB 3.0	Port	2 External USB Port
	1	USB3.0 (left Side)
	2	None
	3	None
	4	None

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Ivy Bridge:
1.5GHz GT2 ES2 QBP8: SA00005AZ10 (4619HZ32L01)
1.5GHz ES2 QBTP: SA00005AZ20(4619HZ32L02)

Pin Assignment Diagram for Intel Ivy Bridge BGA 1023

Legend:

- CPU
- GPU
- PCI Express
- SATA
- USB

Pin Assignments:

Signal	Package Pin	Signal	Package Pin
DM1_RX[0]	M2	FDI0_TX[0]	U7
DM1_RX[1]	P6	FDI0_TX[1]	W1
DM1_RX[2]	P1	FDI0_TX[2]	W1
DM1_RX[3]	P10	FDI0_TX[3]	W6
DM1_RX[4]	N3	FDI0_TX[4]	W6
DM1_RX[5]	P7	FDI0_TX[5]	V4
DM1_RX[6]	P3	FDI0_TX[6]	Y2
DM1_RX[7]	P11	FDI0_TX[7]	AC9
DM1_RX[8]	K1	FDI0_TX[8]	U6
DM1_RX[9]	M8	FDI0_TX[9]	W3
DM1_RX[10]	N4	FDI0_TX[10]	AA7
DM1_RX[11]	R2	FDI0_TX[11]	W7
DM1_RX[12]	K3	FDI0_TX[12]	T4
DM1_RX[13]	M7	FDI0_TX[13]	AA6
DM1_RX[14]	P4	FDI0_TX[14]	AC9
DM1_RX[15]	T3	FDI0_TX[15]	AA11
DM1_RX[16]	K1	FDI0_TX[16]	AC12
DM1_RX[17]	M8	FDI0_TX[17]	U11
DM1_RX[18]	N4	FDI0_TX[18]	AA10
DM1_RX[19]	R2	FDI0_TX[19]	AG8
DM1_RX[20]	K3	FDI0_TX[20]	AG8
DM1_RX[21]	M7	FDI0_TX[21]	AG8
DM1_RX[22]	P4	FDI0_TX[22]	AG8
DM1_RX[23]	T3	FDI0_TX[23]	AG8
DM1_RX[24]	K1	FDI0_TX[24]	AG8
DM1_RX[25]	M8	FDI0_TX[25]	AG8
DM1_RX[26]	N4	FDI0_TX[26]	AG8
DM1_RX[27]	R2	FDI0_TX[27]	AG8
DM1_RX[28]	K3	FDI0_TX[28]	AG8
DM1_RX[29]	M7	FDI0_TX[29]	AG8
DM1_RX[30]	P4	FDI0_TX[30]	AG8
DM1_RX[31]	T3	FDI0_TX[31]	AG8
DM1_RX[32]	K1	FDI0_TX[32]	AG8
DM1_RX[33]	M8	FDI0_TX[33]	AG8
DM1_RX[34]	N4	FDI0_TX[34]	AG8
DM1_RX[35]	R2	FDI0_TX[35]	AG8
DM1_RX[36]	K3	FDI0_TX[36]	AG8
DM1_RX[37]	M7	FDI0_TX[37]	AG8
DM1_RX[38]	P4	FDI0_TX[38]	AG8
DM1_RX[39]	T3	FDI0_TX[39]	AG8
DM1_RX[40]	K1	FDI0_TX[40]	AG8
DM1_RX[41]	M8	FDI0_TX[41]	AG8
DM1_RX[42]	N4	FDI0_TX[42]	AG8
DM1_RX[43]	R2	FDI0_TX[43]	AG8
DM1_RX[44]	K3	FDI0_TX[44]	AG8
DM1_RX[45]	M7	FDI0_TX[45]	AG8
DM1_RX[46]	P4	FDI0_TX[46]	AG8
DM1_RX[47]	T3	FDI0_TX[47]	AG8
DM1_RX[48]	K1	FDI0_TX[48]	AG8
DM1_RX[49]	M8	FDI0_TX[49]	AG8
DM1_RX[50]	N4	FDI0_TX[50]	AG8
DM1_RX[51]	R2	FDI0_TX[51]	AG8
DM1_RX[52]	K3	FDI0_TX[52]	AG8
DM1_RX[53]	M7	FDI0_TX[53]	AG8
DM1_RX[54]	P4	FDI0_TX[54]	AG8
DM1_RX[55]	T3	FDI0_TX[55]	AG8
DM1_RX[56]	K1	FDI0_TX[56]	AG8
DM1_RX[57]	M8	FDI0_TX[57]	AG8
DM1_RX[58]	N4	FDI0_TX[58]	AG8
DM1_RX[59]	R2	FDI0_TX[59]	AG8
DM1_RX[60]	K3	FDI0_TX[60]	AG8
DM1_RX[61]	M7	FDI0_TX[61]	AG8
DM1_RX[62]	P4	FDI0_TX[62]	AG8
DM1_RX[63]	T3	FDI0_TX[63]	AG8
DM1_RX[64]	K1	FDI0_TX[64]	AG8
DM1_RX[65]	M8	FDI0_TX[65]	AG8
DM1_RX[66]	N4	FDI0_TX[66]	AG8
DM1_RX[67]	R2	FDI0_TX[67]	AG8
DM1_RX[68]	K3	FDI0_TX[68]	AG8
DM1_RX[69]	M7	FDI0_TX[69]	AG8
DM1_RX[70]	P4	FDI0_TX[70]	AG8
DM1_RX[71]	T3	FDI0_TX[71]	AG8
DM1_RX[72]	K1	FDI0_TX[72]	AG8
DM1_RX[73]	M8	FDI0_TX[73]	AG8
DM1_RX[74]	N4	FDI0_TX[74]	AG8
DM1_RX[75]	R2	FDI0_TX[75]	AG8
DM1_RX[76]	K3	FDI0_TX[76]	AG8
DM1_RX[77]	M7	FDI0_TX[77]	AG8
DM1_RX[78]	P4	FDI0_TX[78]	AG8
DM1_RX[79]	T3	FDI0_TX[79]	AG8
DM			

RC1
24.9_0402_1%

<PEG>

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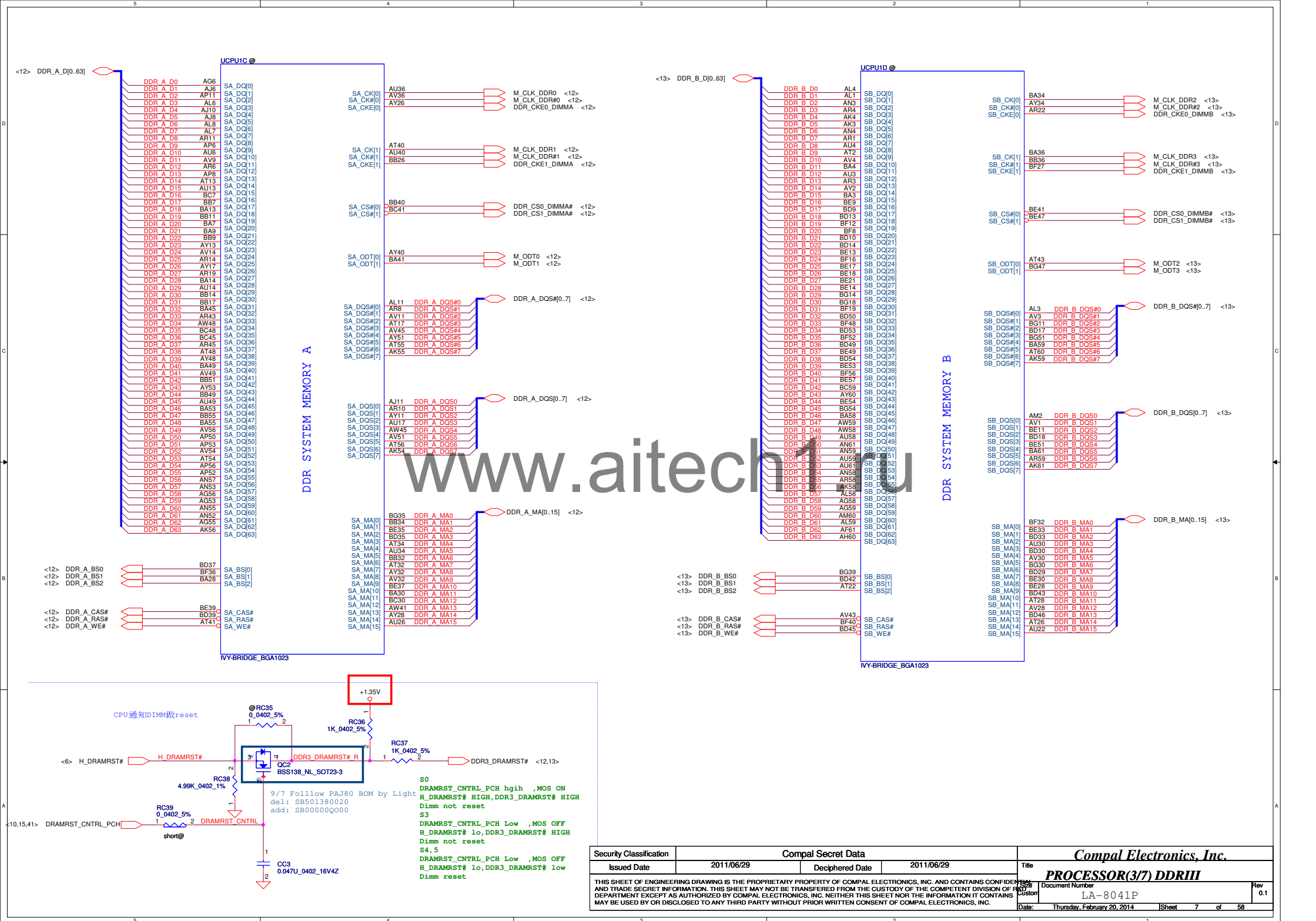
NOTE:eDP_COMPIO and eDP_ICOMPO
should not be left floating even if Internal
Graphic is disabled since they are shared
with other interfaces

<1111> Co-lay eDP function.

↑ 10/05 Change to 0.22uF.

Typ- suggest 220nF. The change in AC capacitor value from 180nF to 265nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

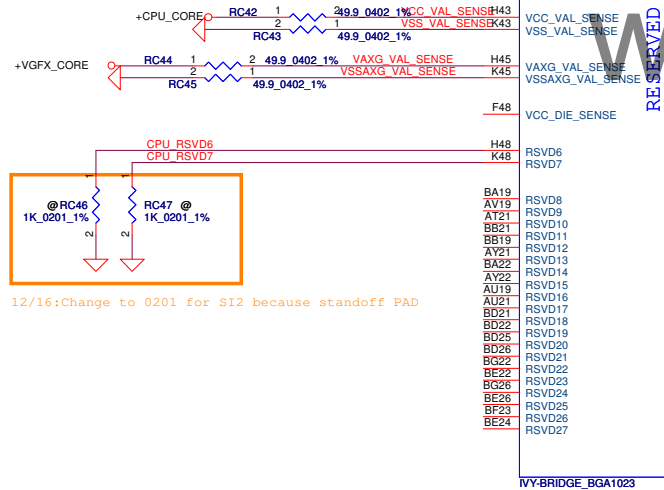
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Change to part G.

Delete T12, T13, T10
12.21

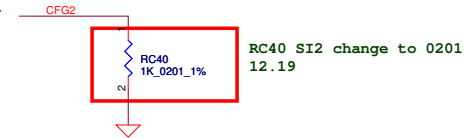
2011.10.18 delete XDP resistor
just reserve test point for XDP.



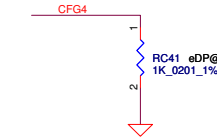
CFG Straps for Processor

PEG bus is reversed, need to PD.

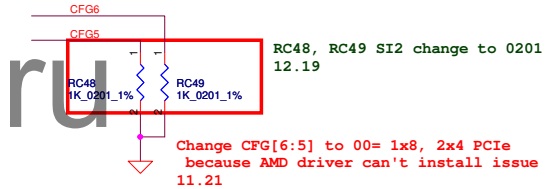
11.01



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

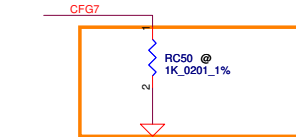


Display Port Presence Strap	
CFG4	* 1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

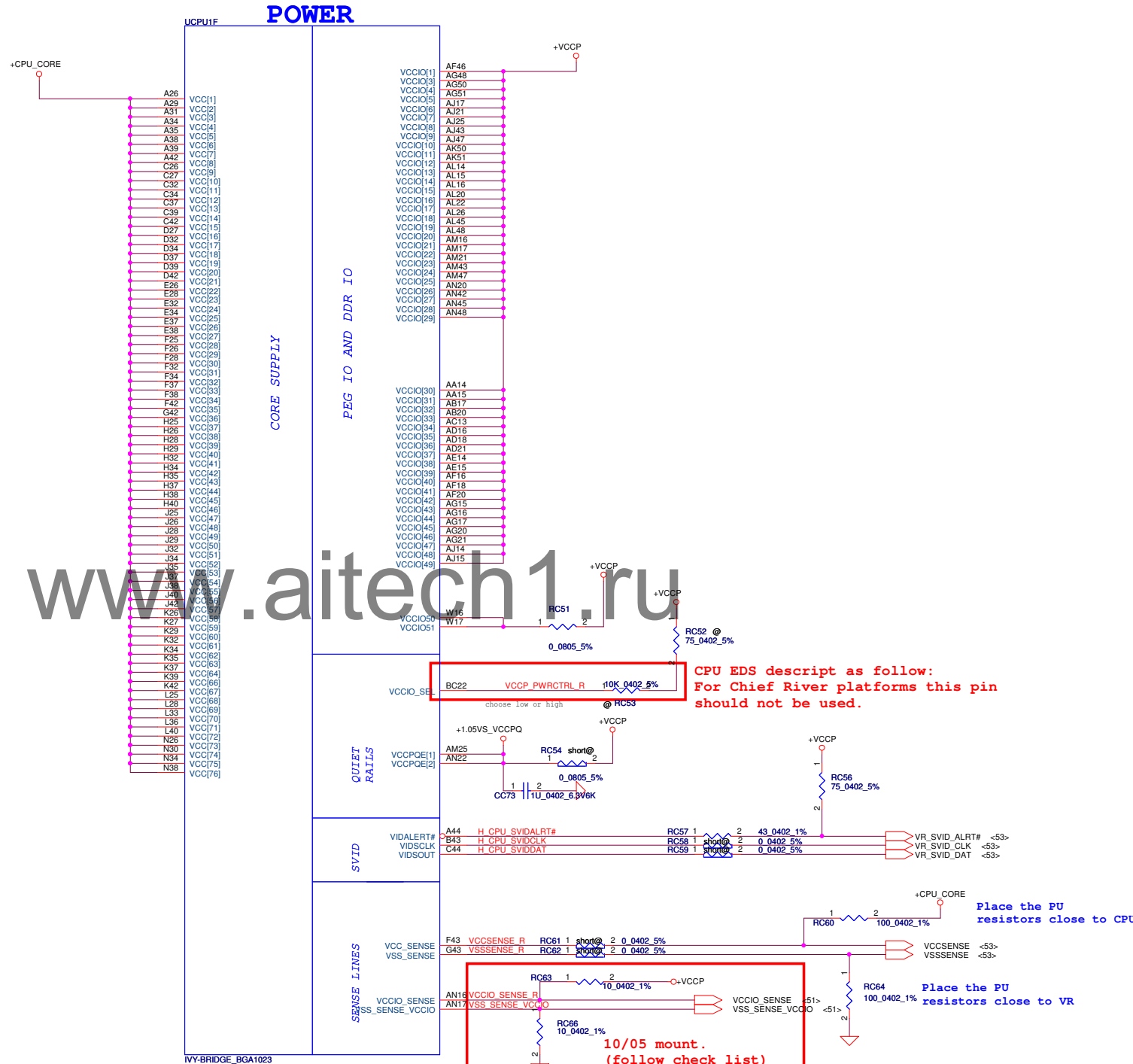


PCIe Port Bifurcation Straps	
CFG[6:5]	* 00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express

12/16: Change to 0201 for SI2 because standoff PAD



PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xRESETB de assertion 0: PEG Wait for BIOS for training



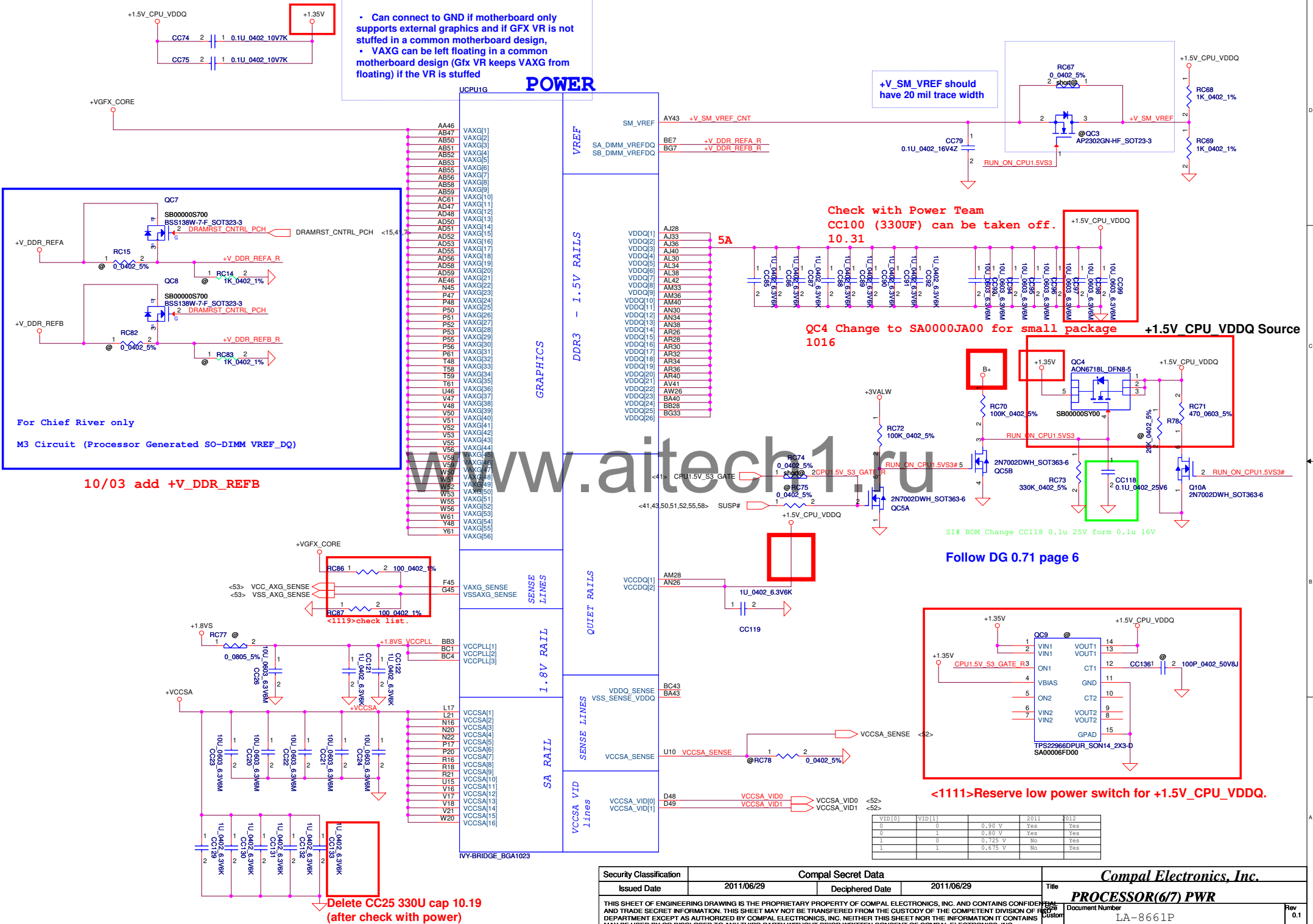
CPU EDS descript as follow:
For Chief River platforms this pin
should not be used.

Place the PU
resistors close to CPU

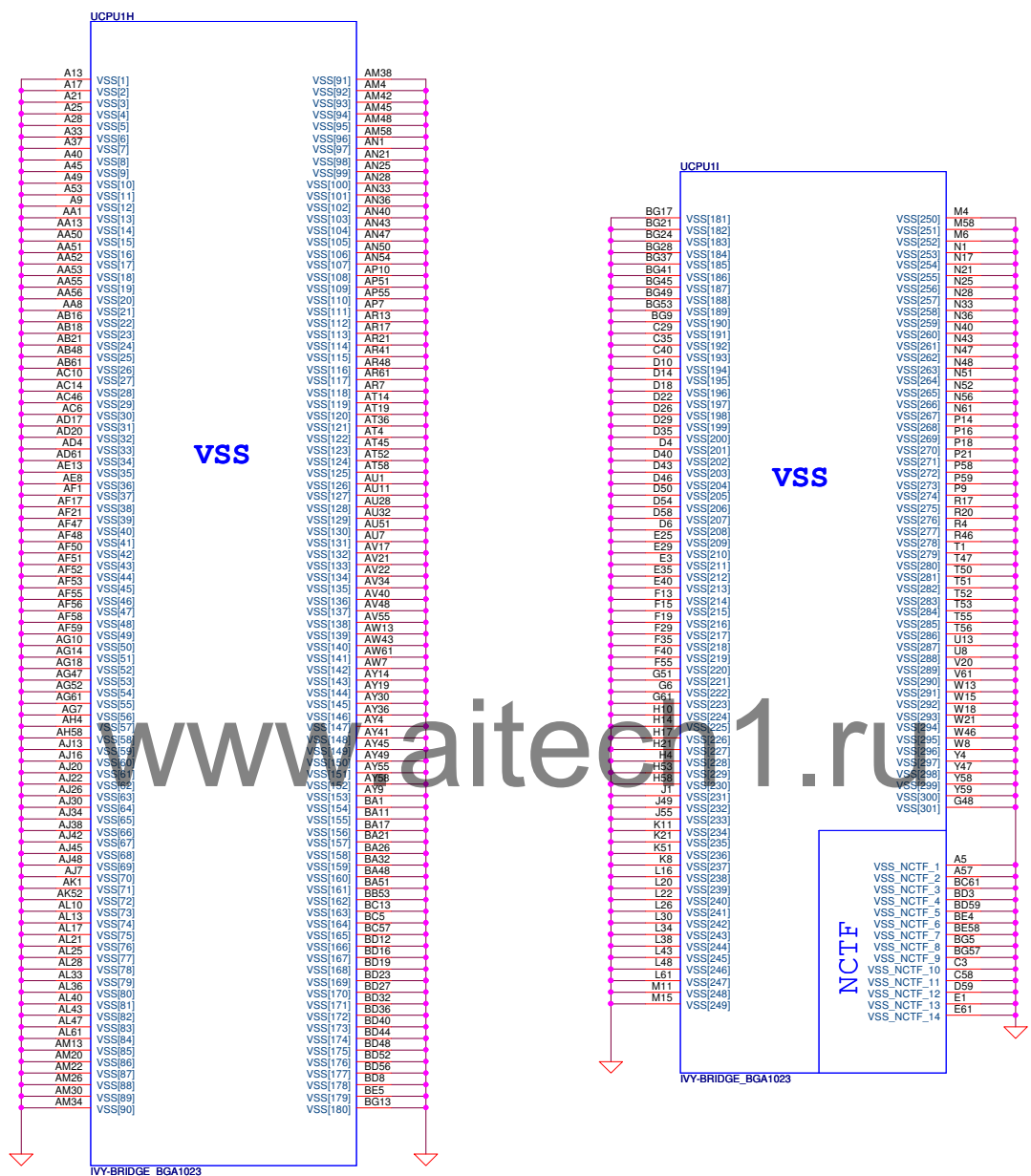
Place the PU
resistors close to VR

10/05 mount.
(follow check list)

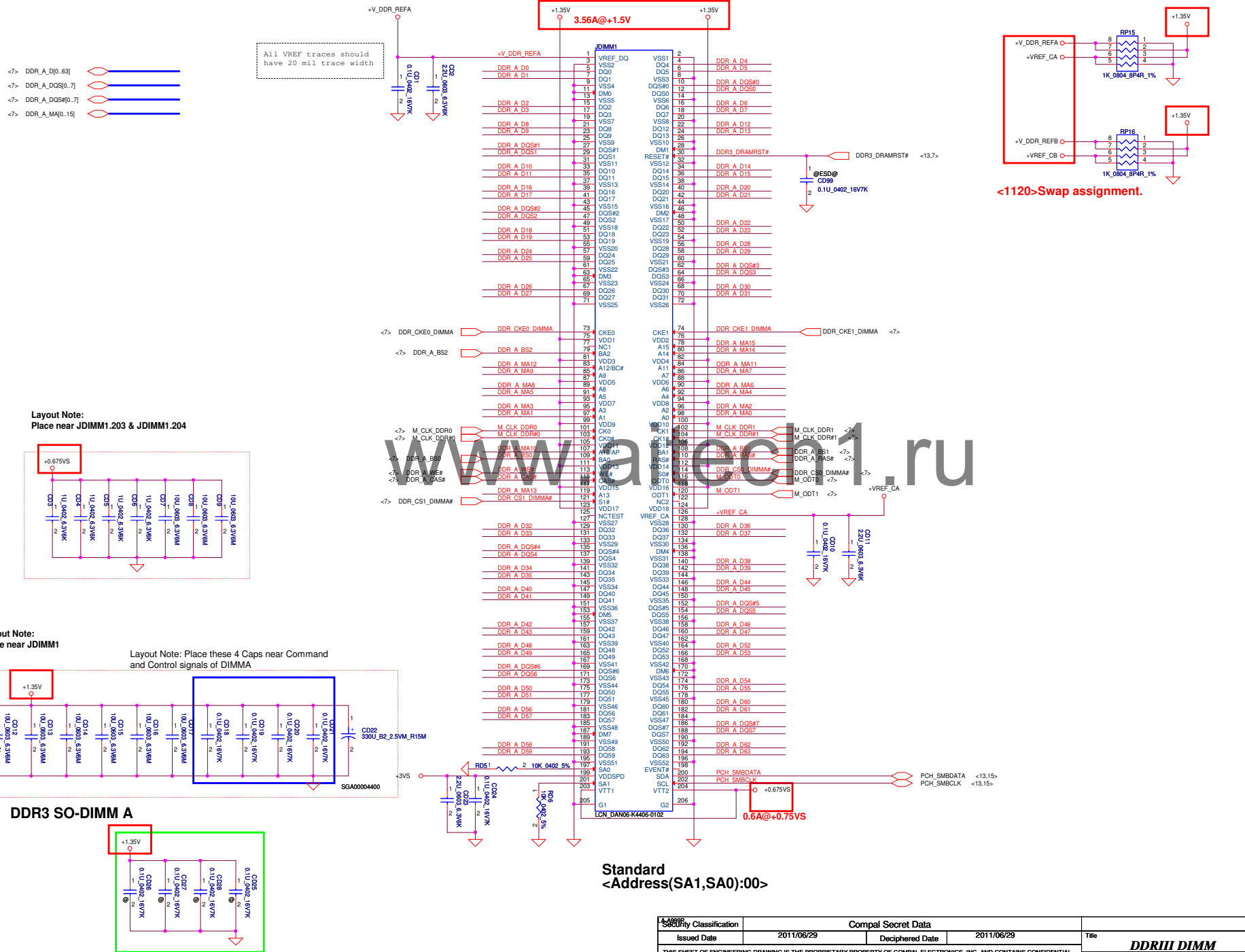
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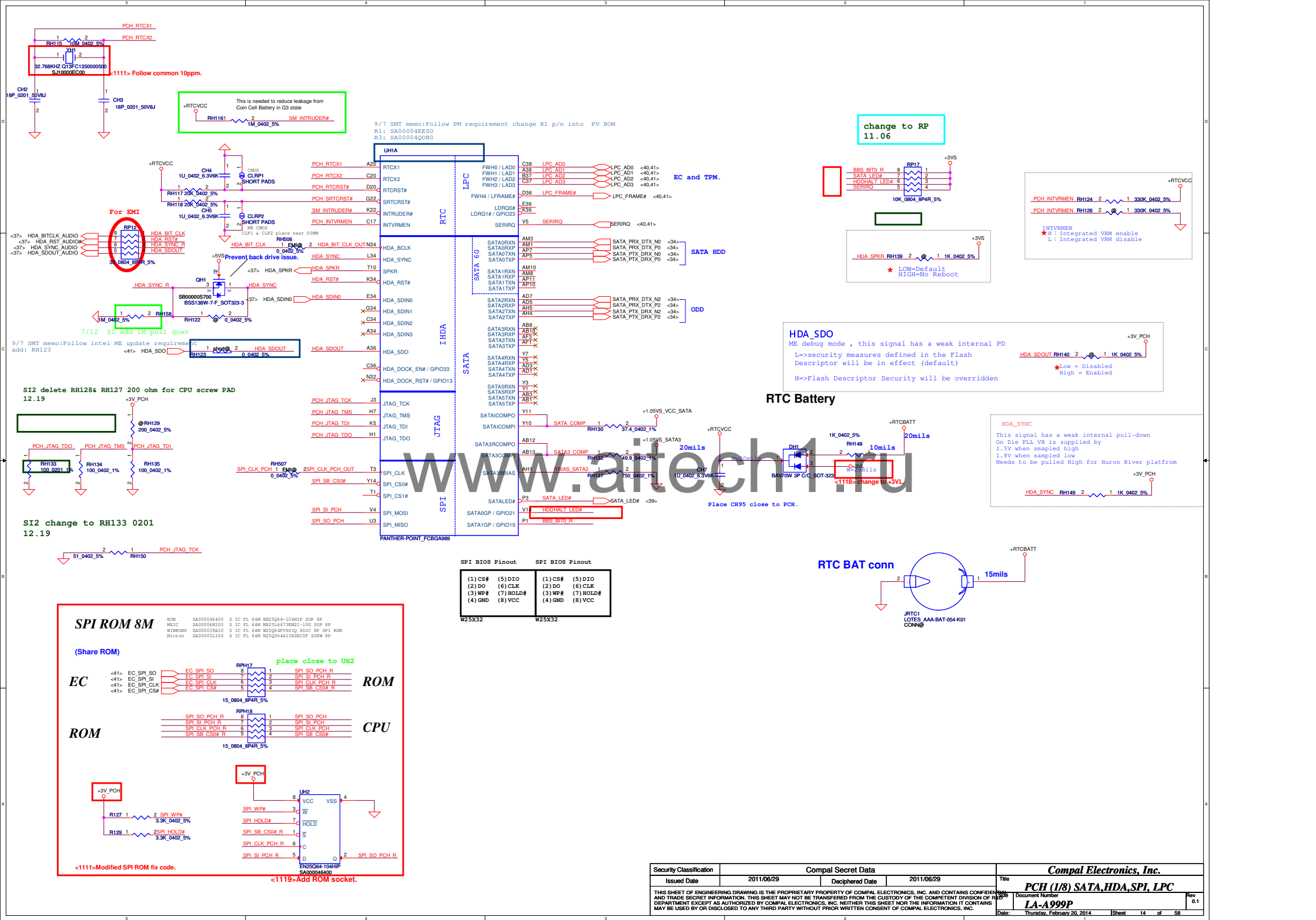
VID[0]	VID[1]		2011	2012
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes



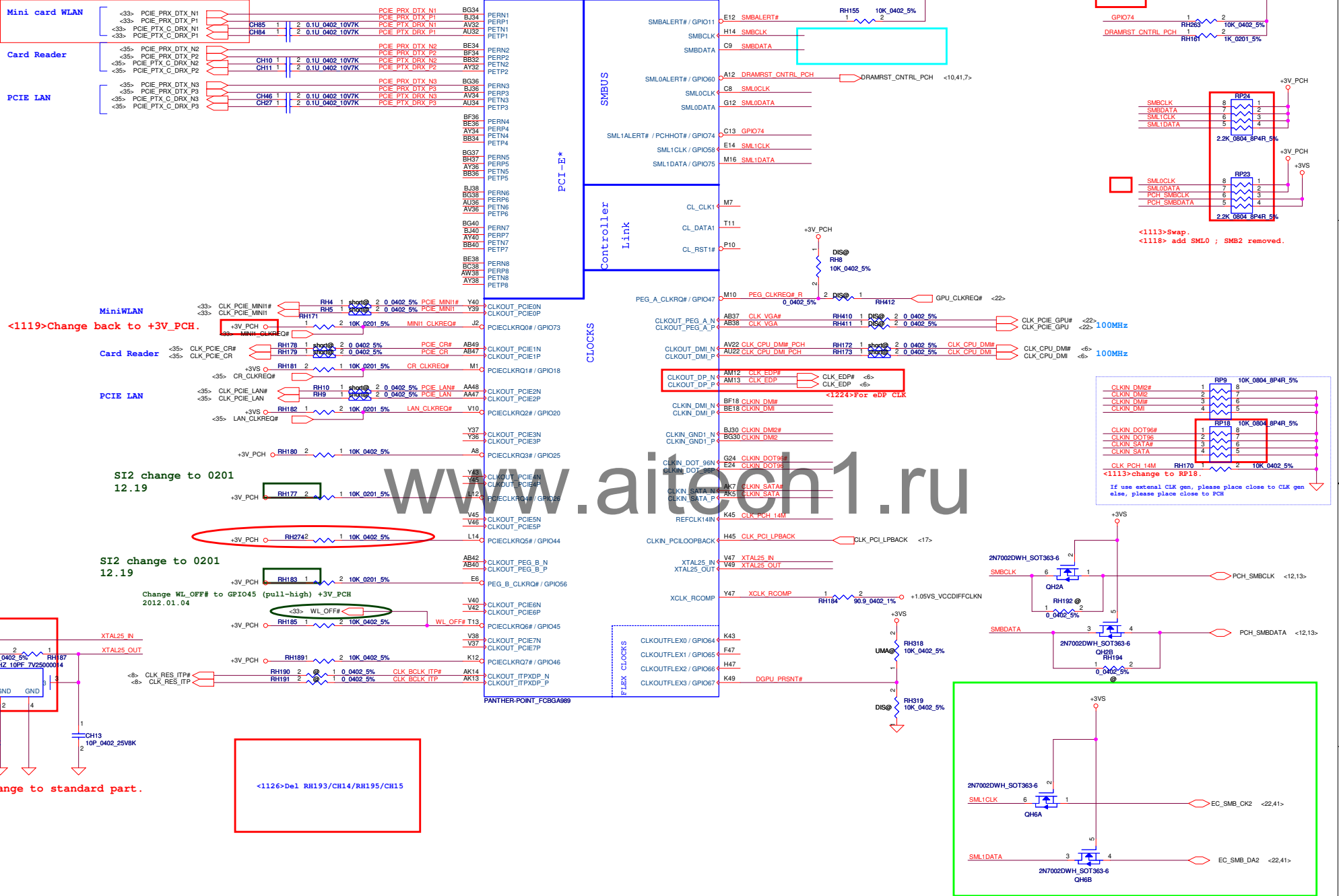
DDR3 SO-DIMM A

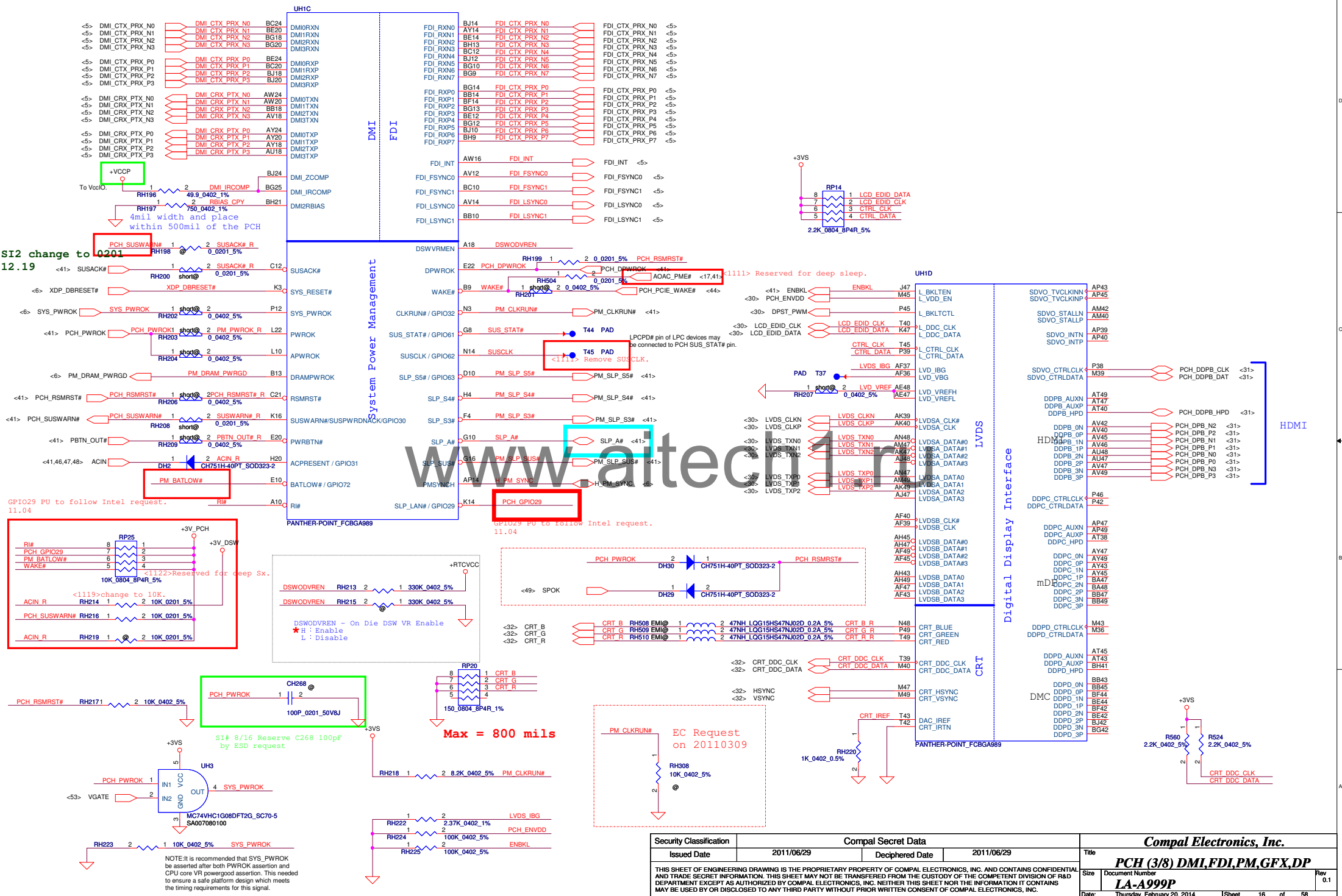


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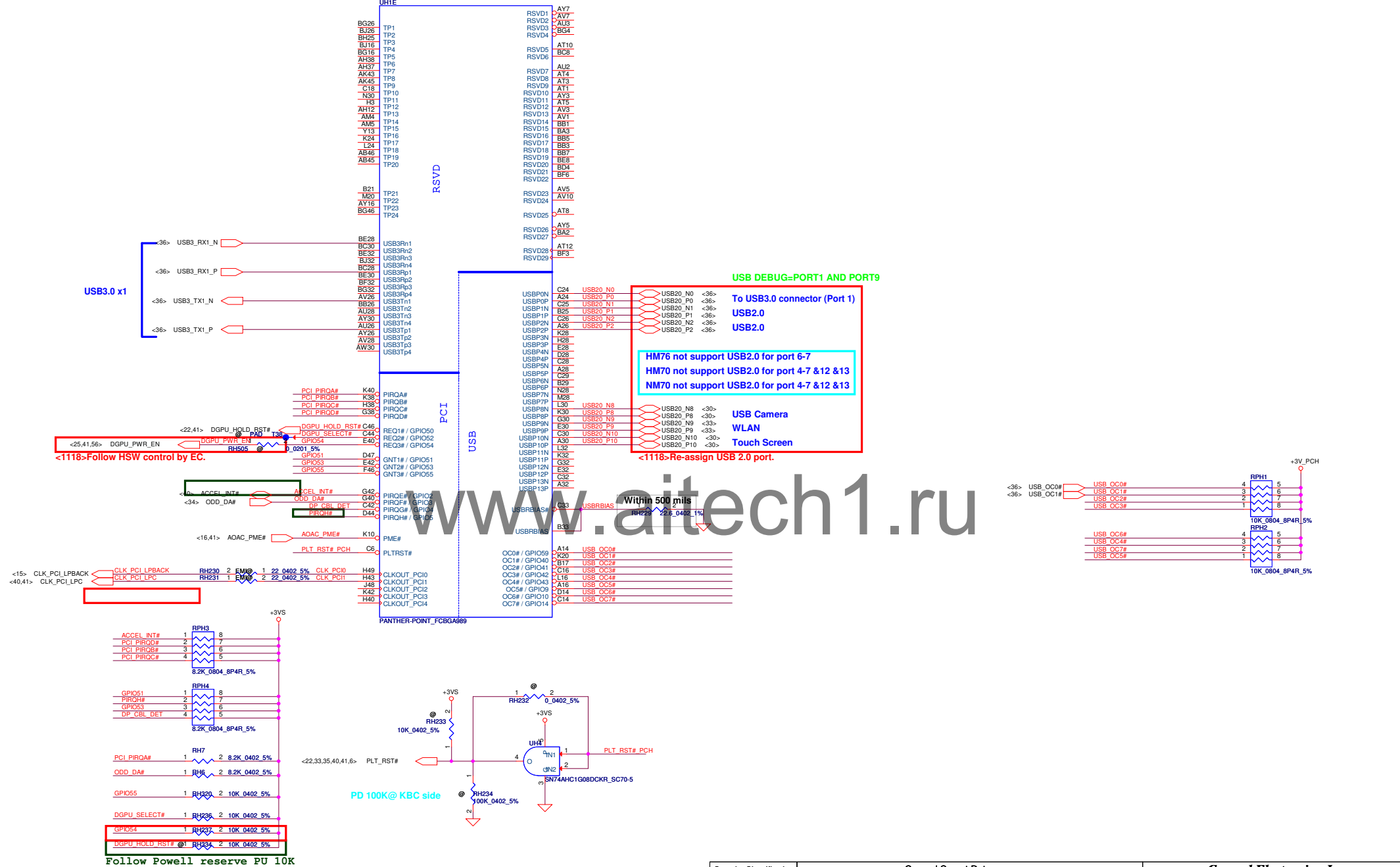


10/03 change to PCIE port1.

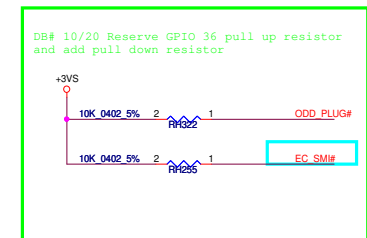




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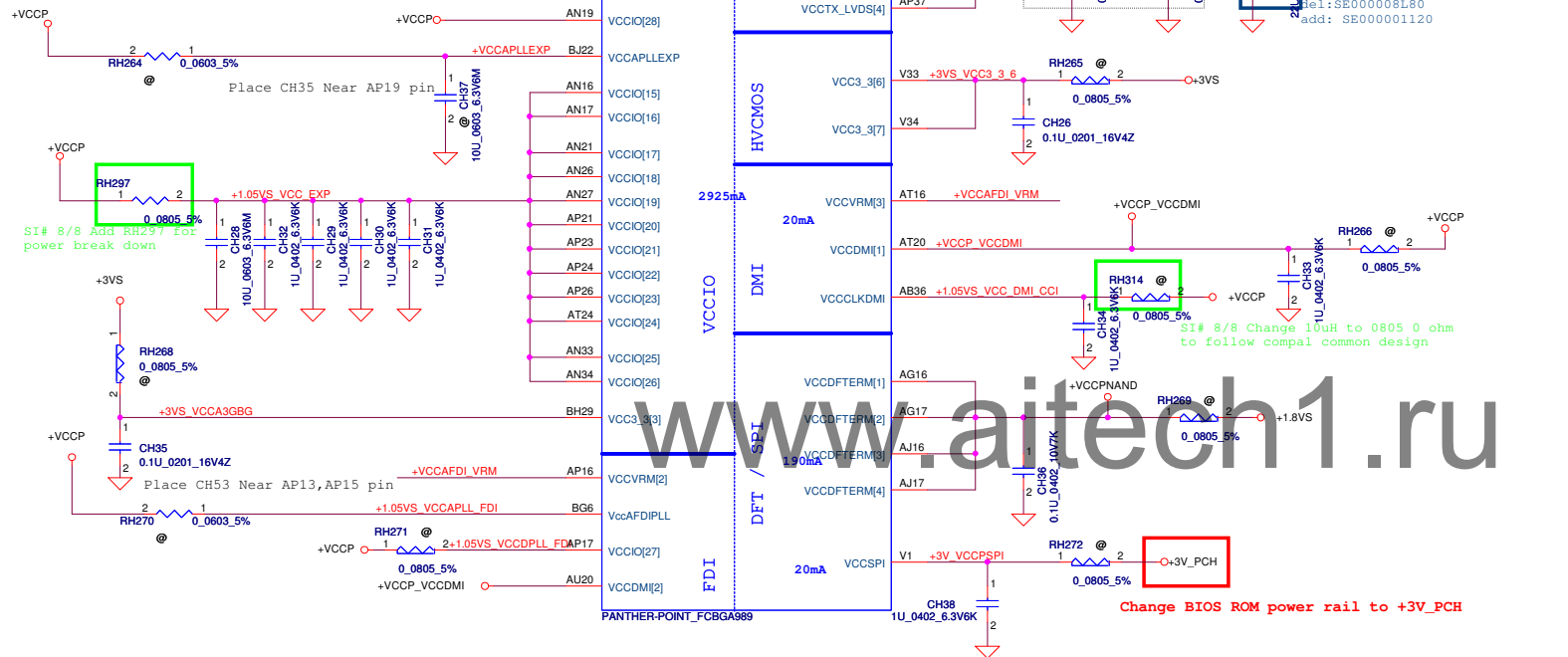


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				Date:	Thursday, February 20, 2014	Sheet 17 of 58

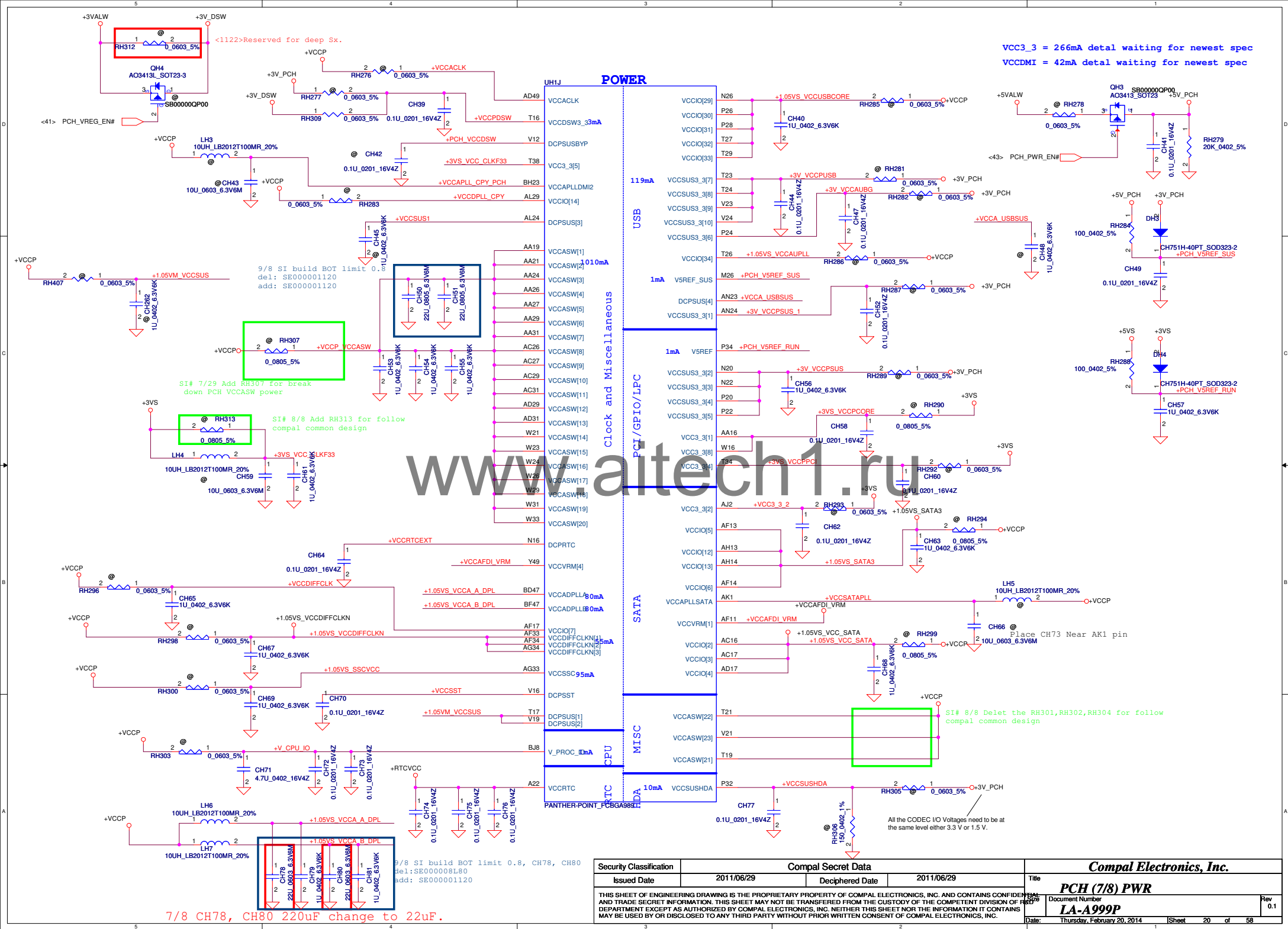


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2011.10.18 change all cap to small size:
22u& 10u to 0603
4.7u to 0402
1u, 0.1u, 0.01u to 0201



PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06



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H5	UH1H	
	VSS[0]	
AA17	VSS[1]	VSS[80] AK38
AA2	VSS[2]	VSS[81] AK4
AA3	VSS[3]	VSS[82] AK42
AA33	VSS[4]	VSS[83] AK46
AA34	VSS[5]	VSS[84] AK8
AB11	VSS[6]	VSS[85] AL16
AB14	VSS[7]	VSS[86] AL17
AB39	VSS[8]	VSS[87] AL19
AB4	VSS[9]	VSS[88] AL2
AB43	VSS[10]	VSS[89] AL21
AB5	VSS[11]	VSS[90] AL23
AB7	VSS[12]	VSS[91] AL26
AC19	VSS[13]	VSS[92] AL27
AC2	VSS[14]	VSS[93] AL31
AC21	VSS[15]	VSS[94] AL34
AC24	VSS[16]	VSS[95] AL48
AC33	VSS[17]	VSS[96] AM11
AC34	VSS[18]	VSS[97] AM14
AD10	VSS[19]	VSS[98] AM36
AD11	VSS[20]	VSS[99] AM39
AD12	VSS[21]	VSS[100] AM43
AD13	VSS[22]	VSS[101] AM45
AD19	VSS[23]	VSS[102] AM46
AD24	VSS[24]	VSS[103] AM7
AD26	VSS[25]	VSS[104] AN2
AD27	VSS[26]	VSS[105] AN29
AD33	VSS[27]	VSS[106] AN3
AD34	VSS[28]	VSS[107] AN31
AD36	VSS[29]	VSS[108] AP12
AD37	VSS[30]	VSS[109] AP19
AD38	VSS[31]	VSS[110] AP28
AD39	VSS[32]	VSS[111] AP30
AD4	VSS[33]	VSS[112] AP32
AD40	VSS[34]	VSS[113] AP38
AD42	VSS[35]	VSS[114] AP4
AD43	VSS[36]	VSS[115] AP42
AD45	VSS[37]	VSS[116] AP46
AD46	VSS[38]	VSS[117] AP8
AD8	VSS[39]	VSS[118] AR2
AE2	VSS[40]	VSS[119] AR48
AE3	VSS[41]	VSS[120] AT11
AF10	VSS[42]	VSS[121] AT13
AF12	VSS[43]	VSS[122] AT18
AD14	VSS[44]	VSS[123] AT22
AD16	VSS[45]	VSS[124] AT26
AF16	VSS[46]	VSS[125] AT28
AF19	VSS[47]	VSS[126] AT30
AF24	VSS[48]	VSS[127] AT32
AF26	VSS[49]	VSS[128] AT34
AF27	VSS[50]	VSS[129] AT39
AF29	VSS[51]	VSS[130] AT42
AF31	VSS[52]	VSS[131] AT46
AF38	VSS[53]	VSS[132] AT7
AF4	VSS[54]	VSS[133] AU24
AF42	VSS[55]	VSS[134] AU30
AF46	VSS[56]	VSS[135] AV16
AF5	VSS[57]	VSS[136] AV20
AF7	VSS[58]	VSS[137] AV24
AF8	VSS[59]	VSS[138] AV30
AG19	VSS[60]	VSS[139] AV38
AG2	VSS[61]	VSS[140] AV4
AG31	VSS[62]	VSS[141] AV43
AG48	VSS[63]	VSS[142] AV8
AH11	VSS[64]	VSS[143] AW14
AH3	VSS[65]	VSS[144] AW18
AH36	VSS[66]	VSS[145] AW2
AH39	VSS[67]	VSS[146] AW22
AH40	VSS[68]	VSS[147] AW26
AH42	VSS[69]	VSS[148] AW28
AH46	VSS[70]	VSS[149] AW32
AH7	VSS[71]	VSS[150] AW34
AJ19	VSS[72]	VSS[151] AW36
AJ21	VSS[73]	VSS[152] AW40
AJ24	VSS[74]	VSS[153] AW48
AJ33	VSS[75]	VSS[154] AV11
AJ34	VSS[76]	VSS[155] AY12
AK12	VSS[77]	VSS[156] AY22
AK3	VSS[78]	VSS[157] AY28
	VSS[79]	VSS[158]

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UH1		
AY4	VSS[159]	VSS[259] H46
AY42	VSS[160]	VSS[260] K18
AY46	VSS[161]	VSS[261] K26
AY8	VSS[162]	VSS[262] K39
B11	VSS[163]	VSS[263] K46
B15	VSS[164]	VSS[264] K7
B19	VSS[165]	VSS[265] L18
B23	VSS[166]	VSS[266] L2
B27	VSS[167]	VSS[267] L26
B31	VSS[168]	VSS[268] L28
B35	VSS[169]	VSS[269] L36
B39	VSS[170]	VSS[270] L48
B7	VSS[171]	VSS[271] M12
F45	VSS[172]	VSS[272] P16
BB12	VSS[173]	VSS[273] M18
BB16	VSS[174]	VSS[274] M22
BB20	VSS[175]	VSS[275] M24
BB22	VSS[176]	VSS[276] M30
BB24	VSS[177]	VSS[277] M32
BB28	VSS[178]	VSS[278] M34
BB30	VSS[179]	VSS[279] M38
BB38	VSS[180]	VSS[280] M4
BB4	VSS[181]	VSS[281] M42
BB46	VSS[182]	VSS[282] M46
BC14	VSS[183]	VSS[283] M6
BC18	VSS[184]	VSS[284] N18
BC2	VSS[185]	VSS[285] P30
BC22	VSS[186]	VSS[286] N47
BC26	VSS[187]	VSS[287] P11
BC32	VSS[188]	VSS[288] P18
BC34	VSS[189]	VSS[289] T33
BC36	VSS[190]	VSS[290] P40
BC40	VSS[191]	VSS[291] P43
BC42	VSS[192]	VSS[292] P47
BC46	VSS[193]	VSS[293] P7
BD46	VSS[194]	VSS[294] R2
BD5	VSS[195]	VSS[295] R48
BE22	VSS[196]	VSS[296] T12
BE38	VSS[197]	VSS[297] T31
BE40	VSS[198]	VSS[298] T37
BF10	VSS[199]	VSS[299] T4
BF12	VSS[200]	VSS[300] W34
BF16	VSS[201]	VSS[301] T46
BF20	VSS[202]	VSS[302] T47
BF22	VSS[203]	VSS[303] T8
BF24	VSS[204]	VSS[304] V11
BF26	VSS[205]	VSS[305] V17
BF28	VSS[206]	VSS[306] V26
BD3	VSS[207]	VSS[307] V27
BF30	VSS[208]	VSS[308] V29
BF38	VSS[209]	VSS[309] V31
BF40	VSS[210]	VSS[310] V36
BF8	VSS[211]	VSS[311] V39
BG17	VSS[212]	VSS[312] V43
BG23	VSS[213]	VSS[313] V7
BG33	VSS[214]	VSS[314] W17
BG44	VSS[215]	VSS[315] W19
BG8	VSS[216]	VSS[316] W2
BH11	VSS[217]	VSS[317] W27
BH15	VSS[218]	VSS[318] W48
BH17	VSS[219]	VSS[319] Y12
BH19	VSS[220]	VSS[320] Y38
H10	VSS[221]	VSS[321] Y4
BH27	VSS[222]	VSS[322] Y42
BH31	VSS[223]	VSS[323] Y46
BH33	VSS[224]	VSS[324] Y8
BH35	VSS[225]	VSS[325] BC29
BH39	VSS[226]	VSS[326] N24
BH43	VSS[227]	VSS[327] AJ3
BH7	VSS[228]	VSS[328] AD47
D3	VSS[229]	VSS[329] B43
D12	VSS[230]	VSS[330] BE10
D16	VSS[231]	VSS[331] BG41
D18	VSS[232]	VSS[332] G14
D22	VSS[233]	VSS[333] H16
D24	VSS[234]	VSS[334] T36
D26	VSS[235]	VSS[335] BC22
D30	VSS[236]	VSS[336] BG24
D32	VSS[237]	VSS[337] C22
D34	VSS[238]	VSS[338] AP13
D38	VSS[239]	VSS[339] M14
D42	VSS[240]	VSS[340] AP3
D8	VSS[241]	VSS[341] BE18
E18	VSS[242]	VSS[342] BC16
E26	VSS[243]	VSS[343] BG28
G18	VSS[244]	VSS[344] BJ28
G20	VSS[245]	
G26	VSS[246]	
G28	VSS[247]	
G36	VSS[248]	
G48	VSS[249]	
H12	VSS[250]	
H18	VSS[251]	
H22	VSS[252]	
H24	VSS[253]	
H26	VSS[254]	
H30	VSS[255]	
H32	VSS[256]	
H34	VSS[257]	
F3	VSS[258]	

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				Rev 0.1

<CPU>

<CPU>

<CPU>

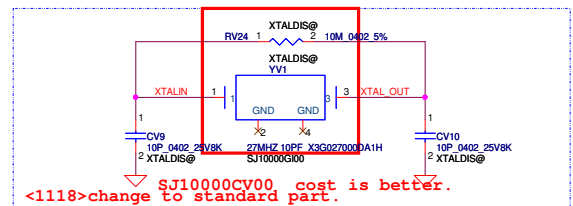
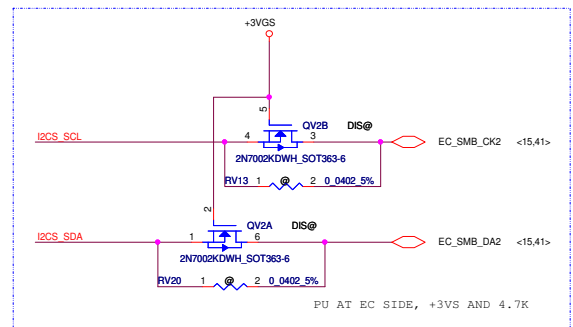
Differential signal

Controlled by EC "AND" PCH

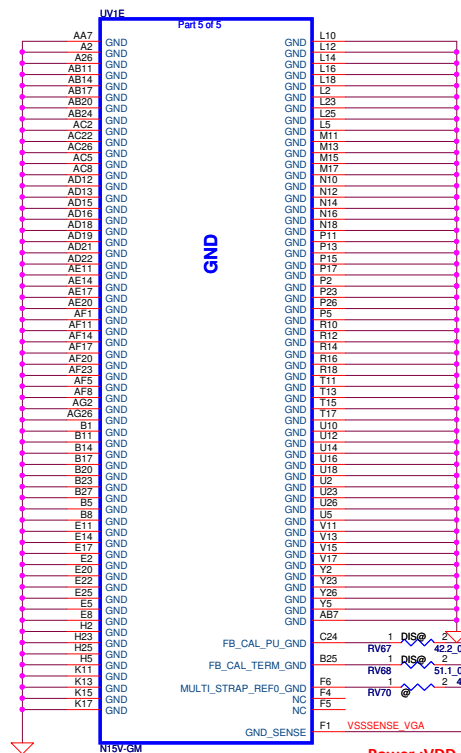
SI 11/05 change RV182.1
change to +3VGS from GPU_PWR_EN

#9/2 , Add RV191 between.
GPU_PWR_LEVEL# and GPU_THERMAL_DET#

#8/19 ,N15V-GM didn't support GC6,
unpop QV13 ,QV14.

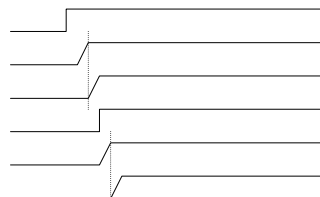


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Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	N15V-GM PCIE/DAC/GPIO
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Power on

DGPU_PWR_EN
+3VGS
+VGA_CORE
DGPU_PWROK
+1.05VGS
+1.5VGS



40us < Rt < 2ms

<18,56> DGPU_PWROK

#08/20 Don't support GC6, Add RV66. Unpop QV16, RV41, RV42, CV78.

#8/19.RV70 unpop, N15V-GM use binary mode.

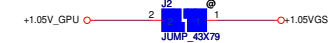
Contrl by power

Power :VDD_SENSE & GND_SENSE
Differential signal

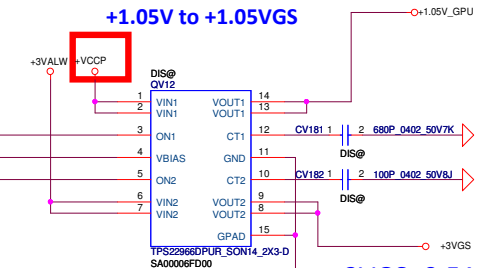
www.aitech1.ru

#8/20 : N15V-GM don't support GC6 function. UV20 unpop.

+1.05VGS=1.6A,4vias.

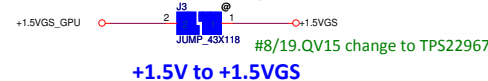


+3VALW to +3VGS
+1.05V to +1.05VGS

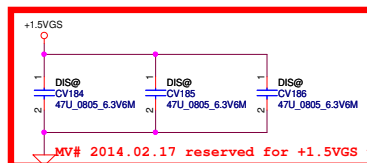
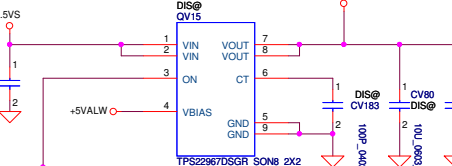


+3VGS=0.5A,2vias.

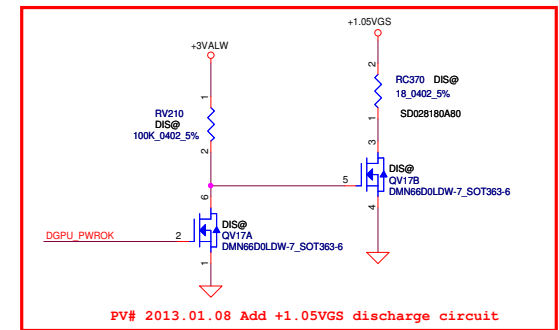
+1.5VGS=3.6A,8vias.



+1.5V to +1.5VGS

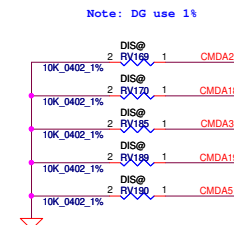


MV# 2014.02.17 reserved for +1.5VGS transient noise.



PV# 2013.01.08 Add +1.05VGS discharge circuit

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	RANK 0	
Address	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	R5T	R5T
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14		
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

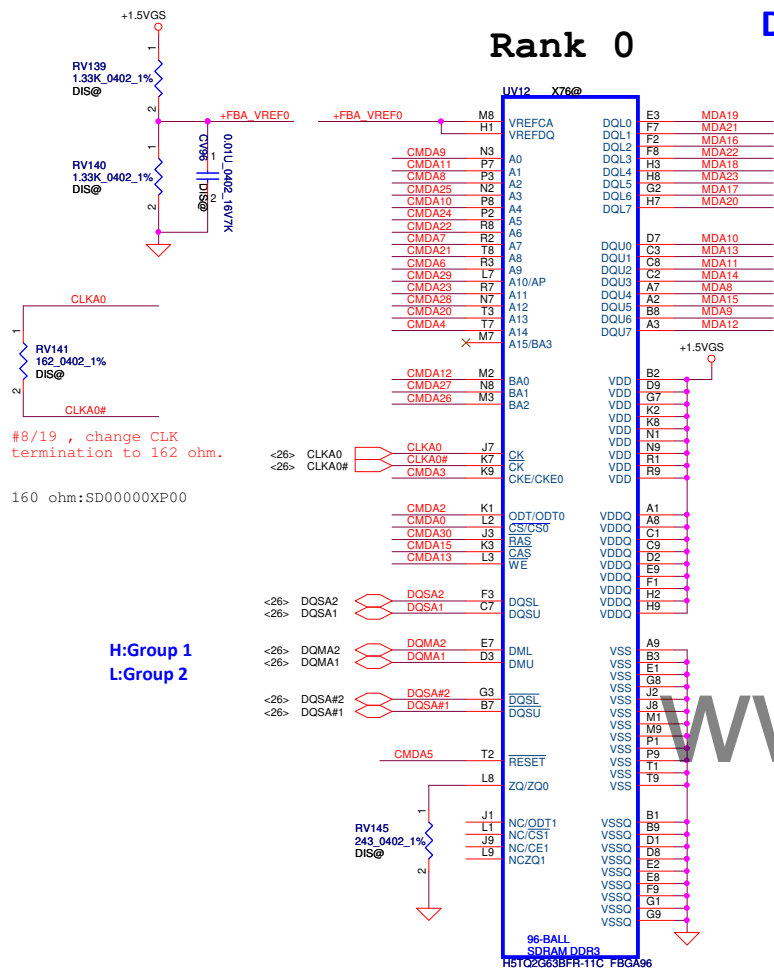
Memory Partition A RANK 0

Data0~Data31

MDA[0..63] <26,28>
CMDA[30..0] <26,28>

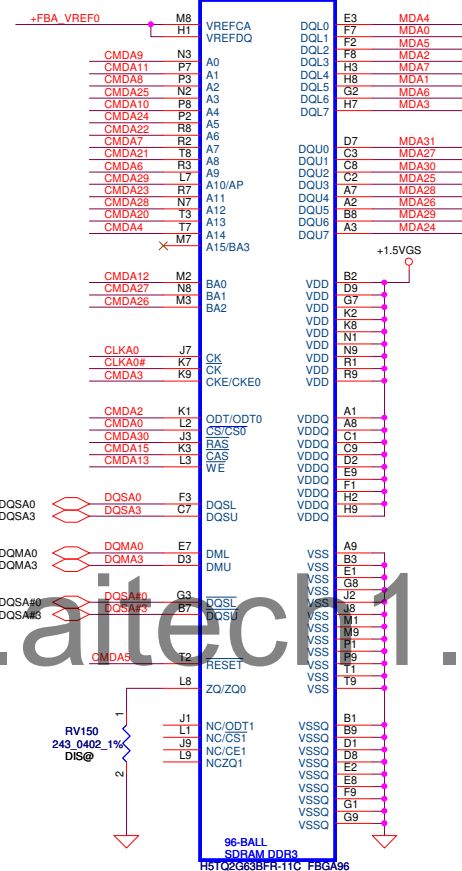
Rank 0

Rank 0



Group 2

Group 1

L:Group 0
H:Group 3

Group 0

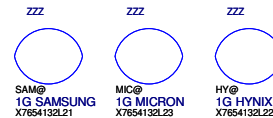
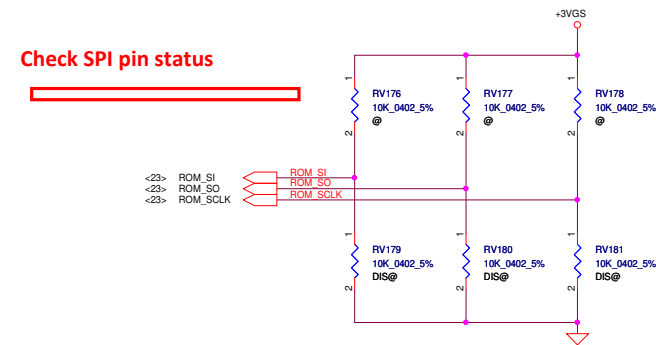
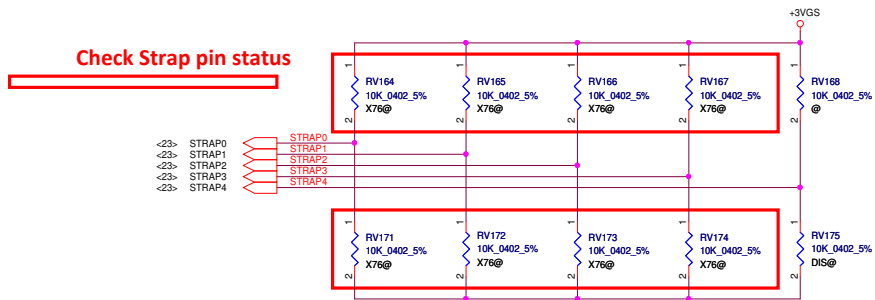
Group 3

Mode D Command Mapping

RANK 0		
Address	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14		
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	N15V-GM VRAM A Lower
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Rank 0



GPU	Project	VRAM size	CH	Description	Compal VRAM P/N	VRAM description	ROM_CFG setup [3...0]	RAM_CFG	R P/N
N15V-GM (23x23) 64bit (One CH single rank)	ZSO40	128M(X16)	CHA	DDR3 Hynix 128Mx16 1.5V	SA00006H400	H5TC2G3FFF-11C 1000MHz	1100	RV171+RV172+RV167+RV166	
	ZSO50	128M(X16)	CHA	DDR3 Micron 128Mx16 1.5V	SA000067500	MT41U128M16JT-093G:K 1000MHz	0001	RV164+RV172+RV173+RV174	
		128M(X16)	CHA	DDR3 Samsung 128Mx16 1.5V	SA000068U00	K4W2G1646E-BC1A 1000MHz	0101	RV164+RV172+RV166+RV174	

#9/5 RAM_CFG follow RVL-06891-001 table 1.
Dule Rank layout with single Rank population.

Table 123

Strap pin Name	Strap Mapping	Resistance	Polarity	Logical Strapping Bit0
ROM_SCLK	SMB_ALT_ADDR	10K	Pull-down to GND.	
ROM_SI	SUB_VENDOR	10K	Pull-down to GND if no VBIOS ROM.	
ROM_SO	VGA_DEVICE	10K	Pull-down to GND(no diaplay).	
STRAP0	RAM_CFG[0]	10K		
STRAP1	RAM_CFG[1]	10K		
STRAP2	RAM_CFG[2]	10K		
STRAP3	RAM_CFG[3]	10K		
STRAP4	PCIE_MAX_SPEED	10K	Pull-down to GND(PCIE Gen1).	

SMBUS_ALT_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

SUB_VENDOR

0	Disable (Default)
1	

VGA_DEVICE

0	Non-Primary 3D Acceleration Device(Class Code 302h)(Default)
1	Primary Display or VGA Device .

PCIE_MAX_SPEED

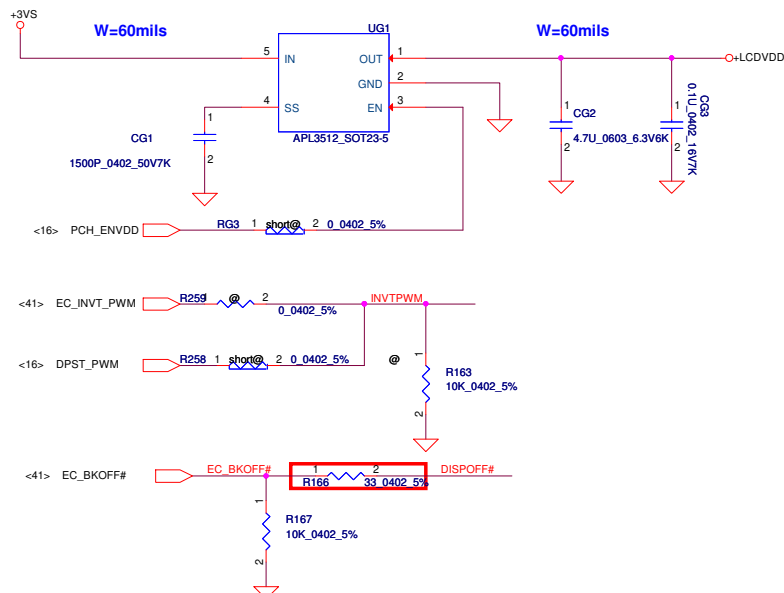
0	Limit to PCIe Gen1
1	PCIe Gen 2/3 Capable

USER Straps

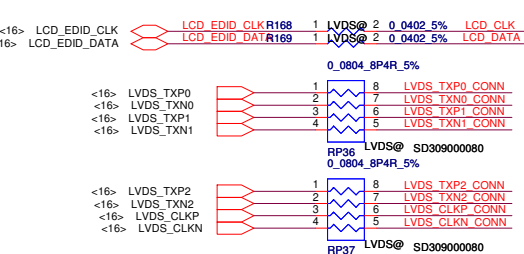
User [3:0]	
1000-1100	Customer defined

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				Date: Thursday, February 20, 2014	Rev 1.0
				Sheet 29 of 58	

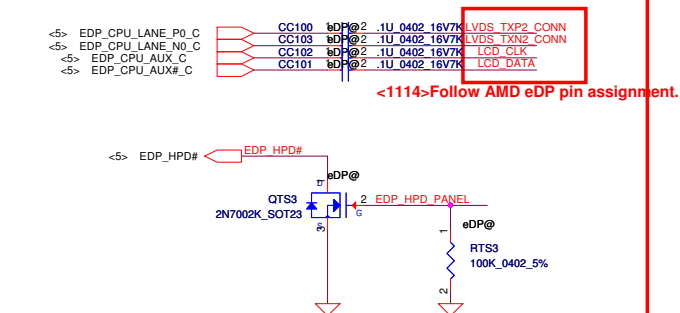
LVDS Power



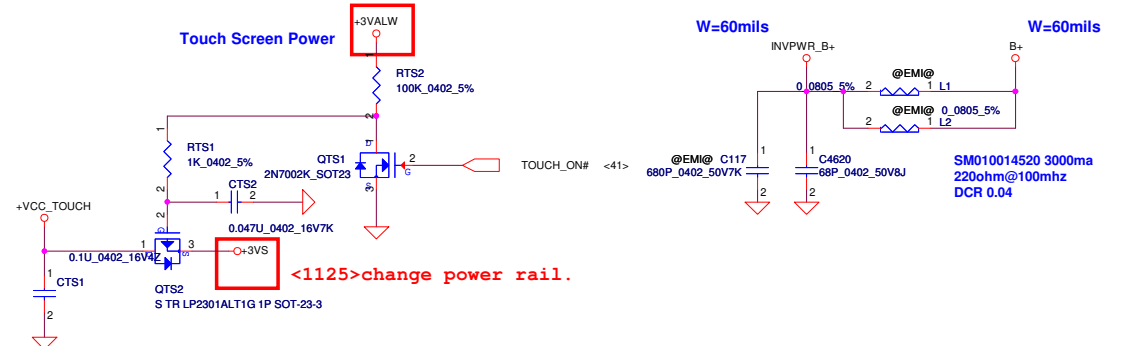
LVDS SKU



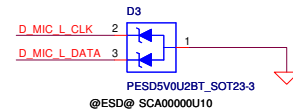
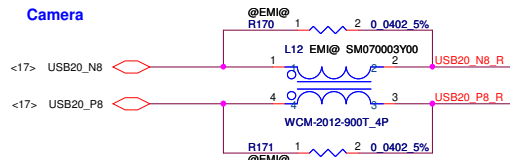
eDP SKU



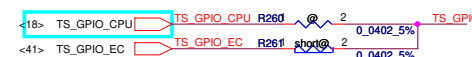
Touch Screen Power



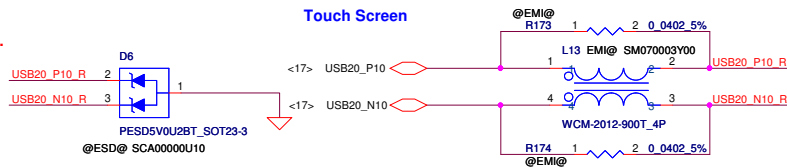
Camera



<DB>LA1/LA2 closed to Audio codec



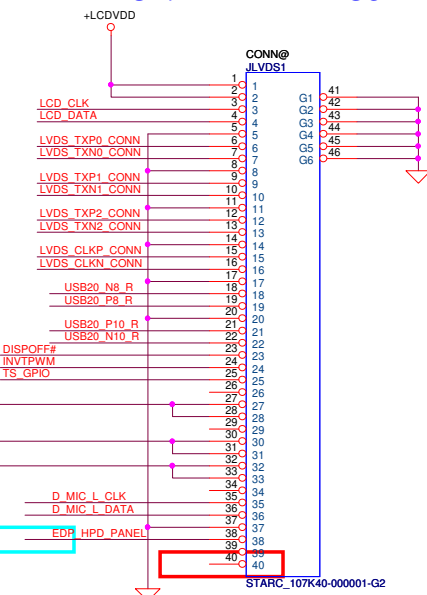
Touch Screen



W=60mils

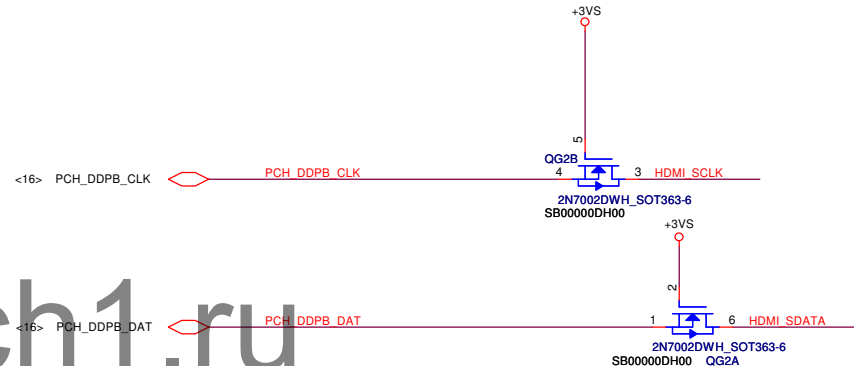
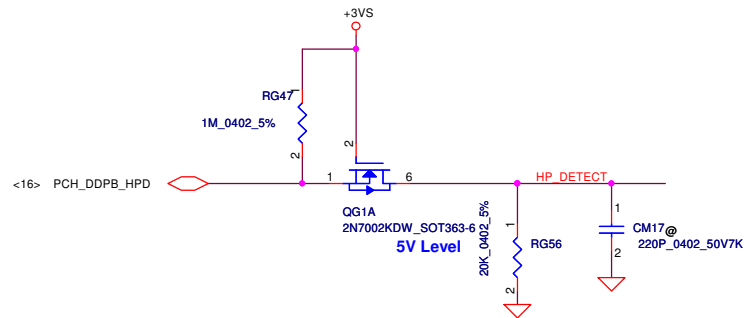
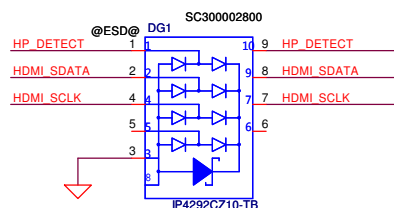
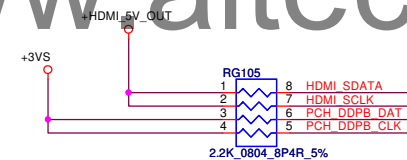
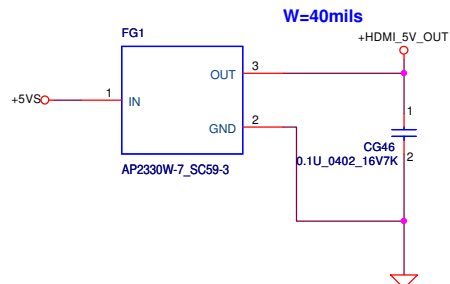
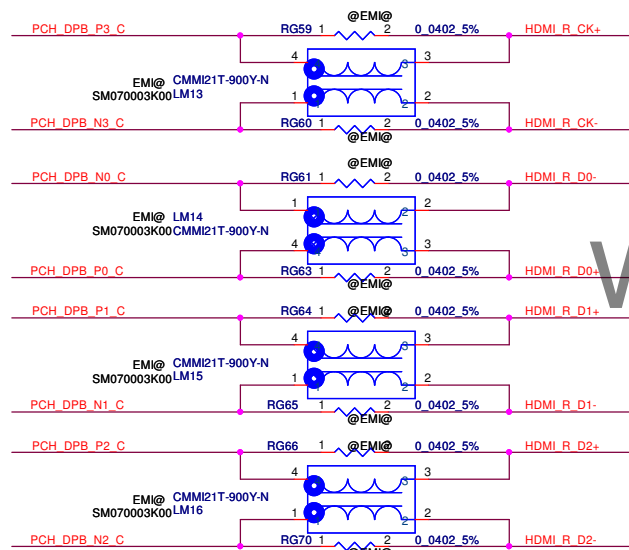
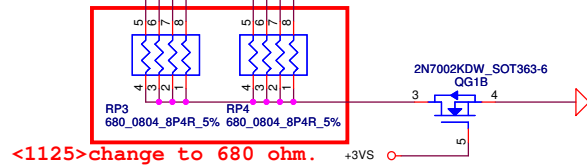
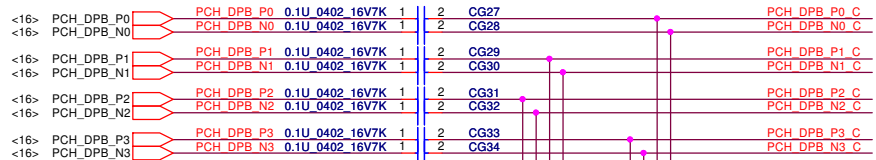
W=60mils

LCD/LED PANEL Conn.

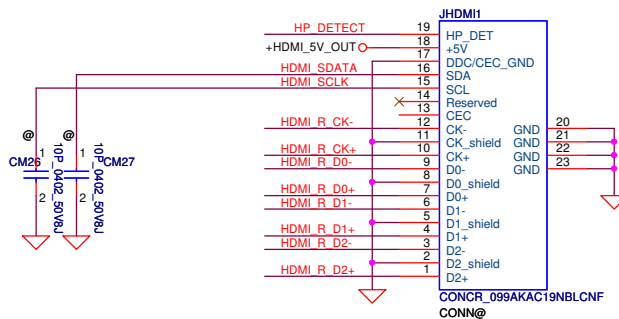


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		Sheet		30		of		58			

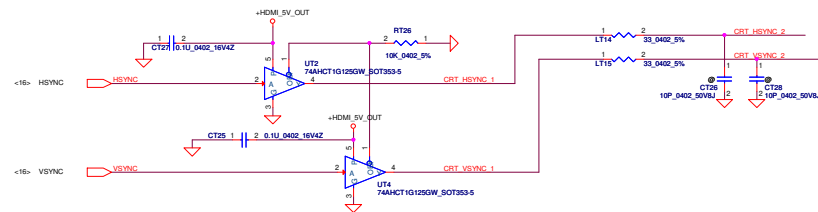
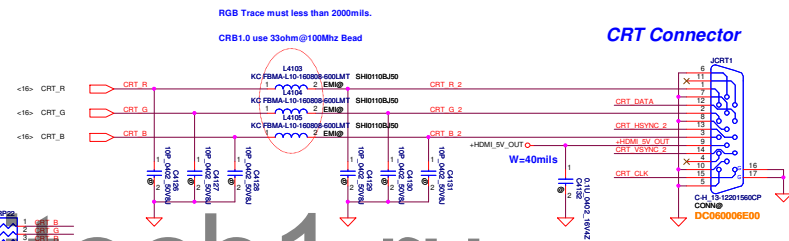
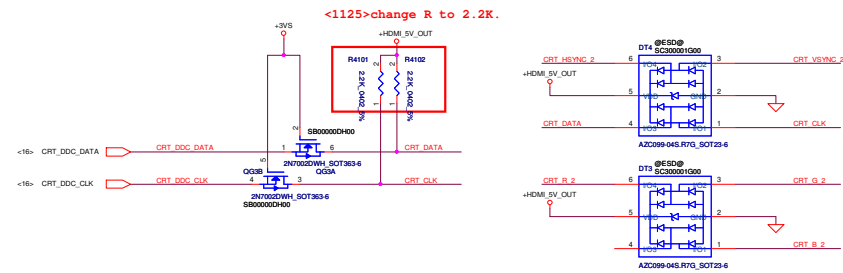
<CPU>



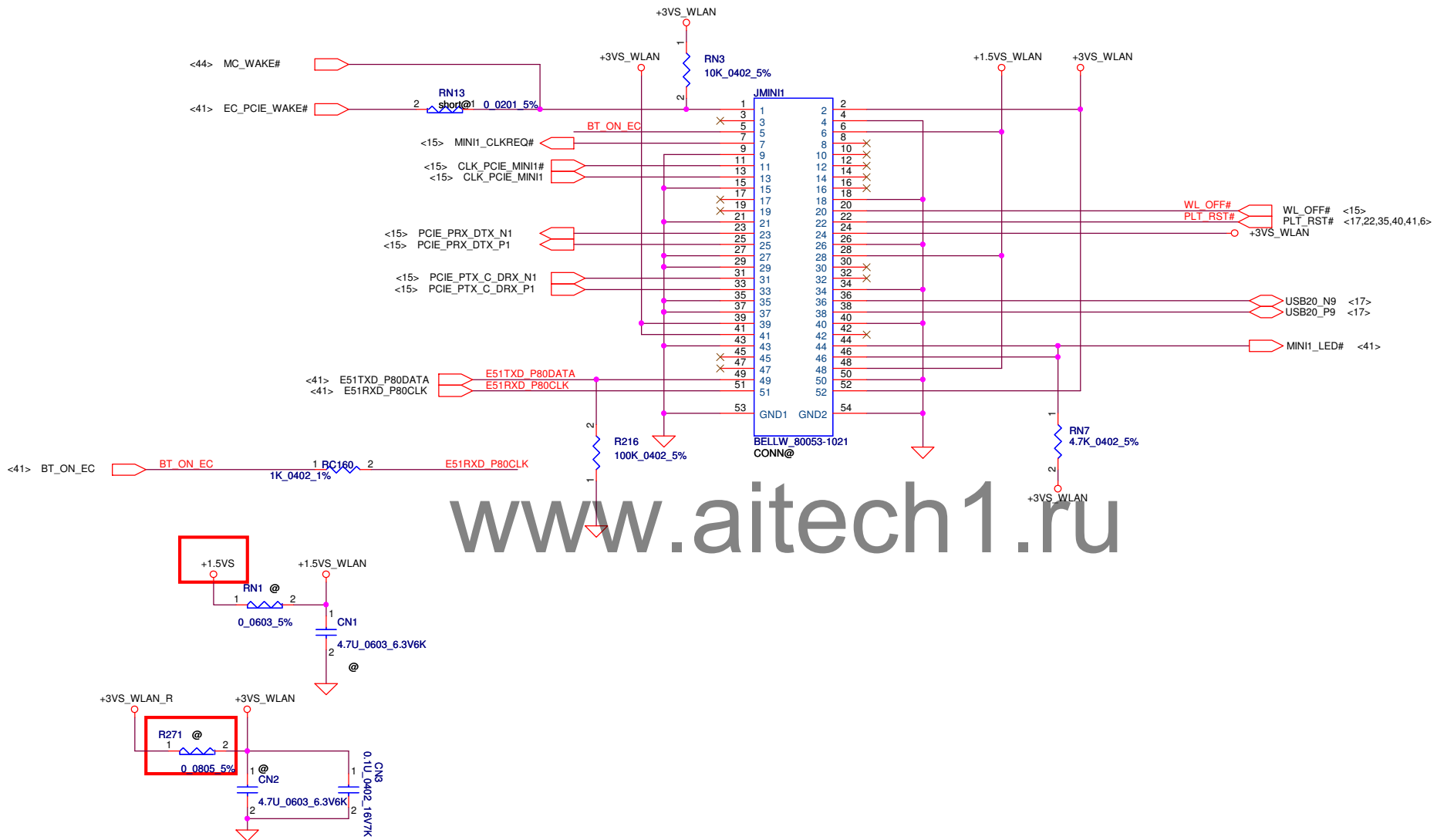
HDMI Conn.



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Date		Thursday, February 20, 2014		Sheet 31 of 58	



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Change	LA-A999P	Doc#	Yurdsly, February 26, 2014	01

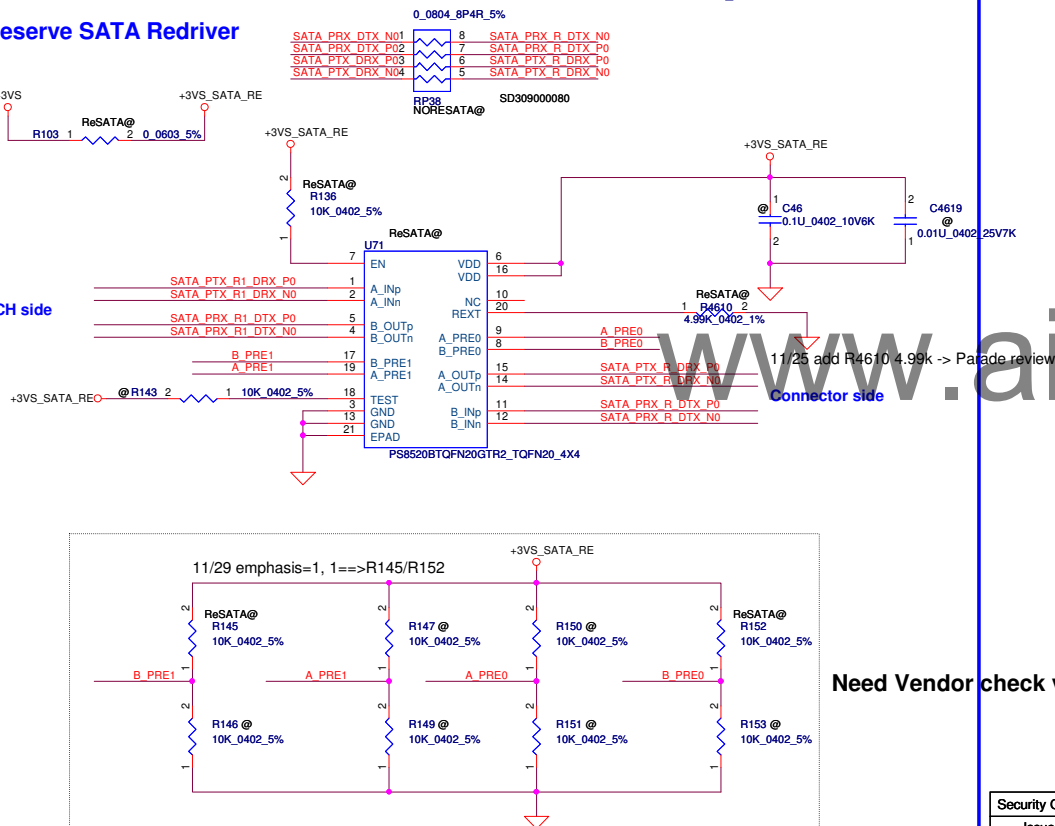


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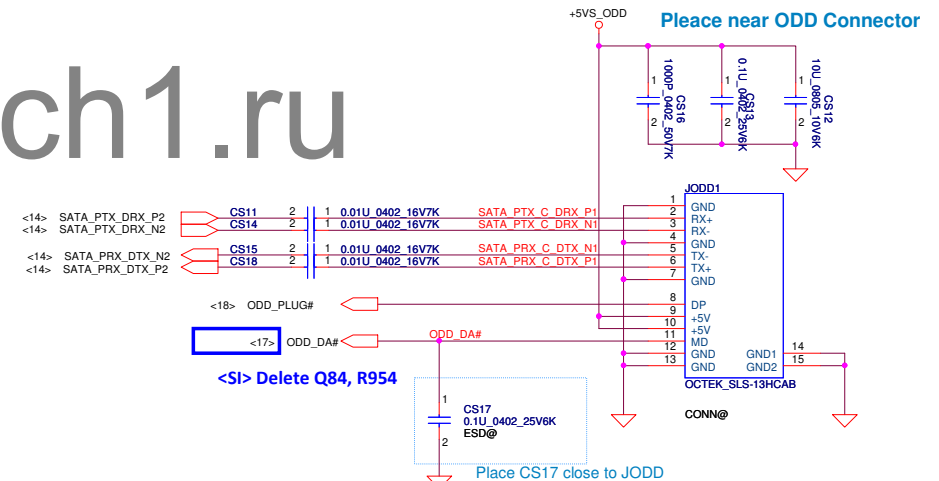
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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	WLAN
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Reserve SATA Redriver



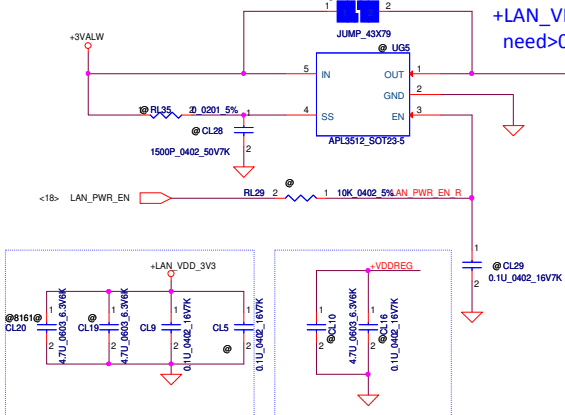
Need Vendor check value



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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	ODD/SATA Conn
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				Date:	Thursday, February 20, 2014
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JHW1 need to short

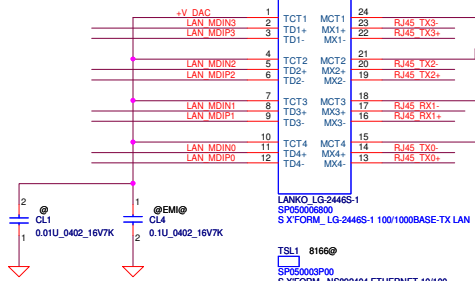
+LAN_VDD_3V3 Rising time need>0.5ms and <100ms



CL9 & CL5 close to UL1: Pin 11,32
CL19 close to UL1: Pin 32
CL20 close to UL1: Pin 11

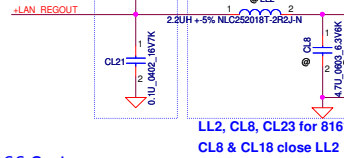
CL10 & CL16 close to UL1: Pin 23

SP050005L00 Footprint

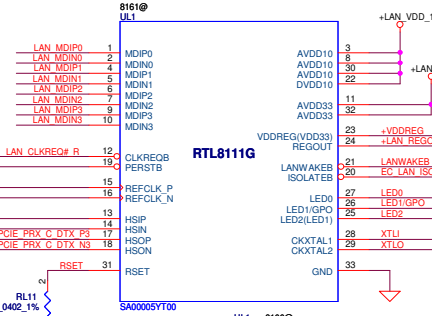


(SP050003P00) 10/100 8166@
(SP050006800) Giga 8161@

RTL8151G (LDO mode)



8151/8166 Co-Lay



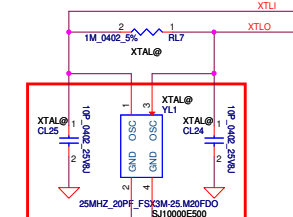
(SA000063500) 10/100 8166@
(SA00005Y100) Giga 8151@

	LDO mode	Switching mode
LL1	SMT	@
CL21	SMT	@
LL2	@	SMT
CL8	@	SMT

CL14 & CL15 close UL1 Pin22
CL26 & CL27 close UL1 Pin30

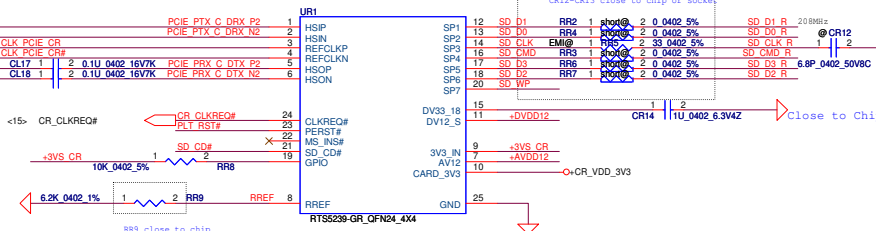
Place CL11-CL13 close UL1 Pin 3, 8, 22

+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil

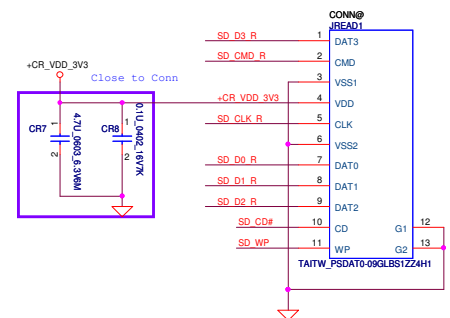


<1118>change to standard part.

RTS5239



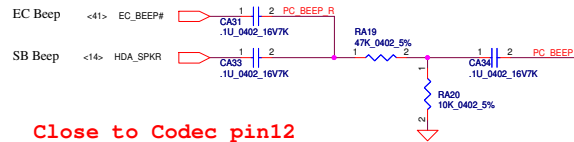
Card Reader Connector



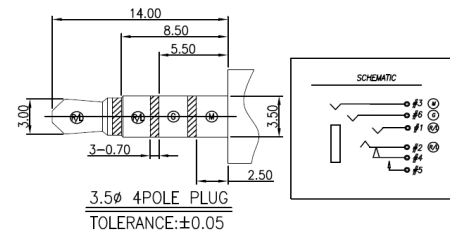
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PC BEEP



Delete ESD Diode



Internal Speaker

Headphone

Internal SPK

<DB>Relace RA13/RA14/RA15/RA16 close to UA1

wide 40 MIL Delete ESD Diode

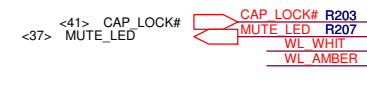
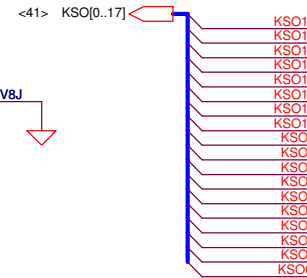
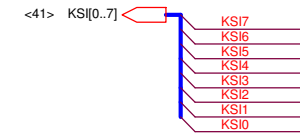
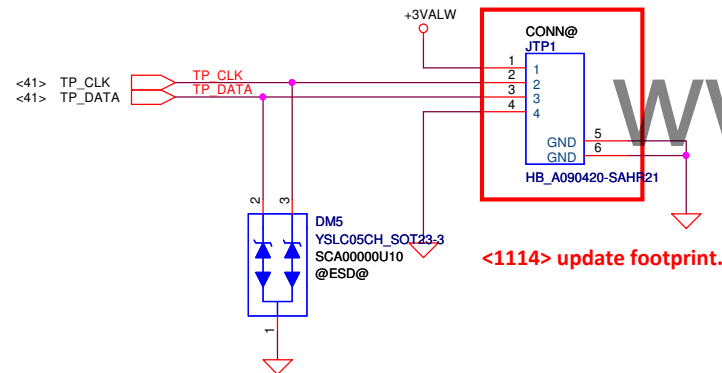
COMBO AUDIO JACK

HPR, HPL, 15mil Keep 30mil

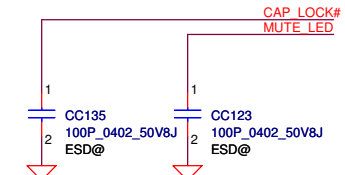
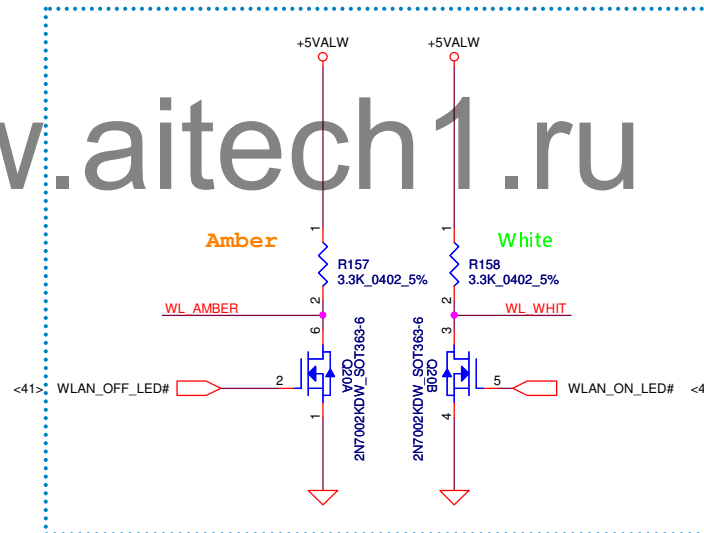
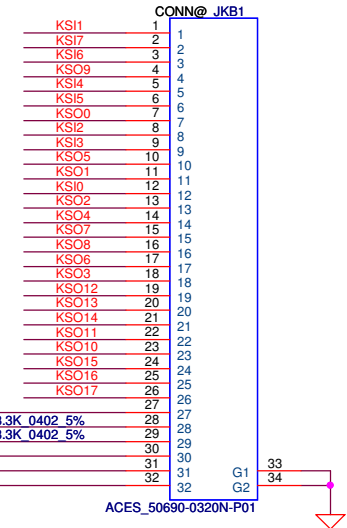
Jack detect
Combo Mic = High
Normal HP = Low

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2013/01/04		2015/01/04		AUDIO ALC259-VC2-CG	
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Touch pad conn

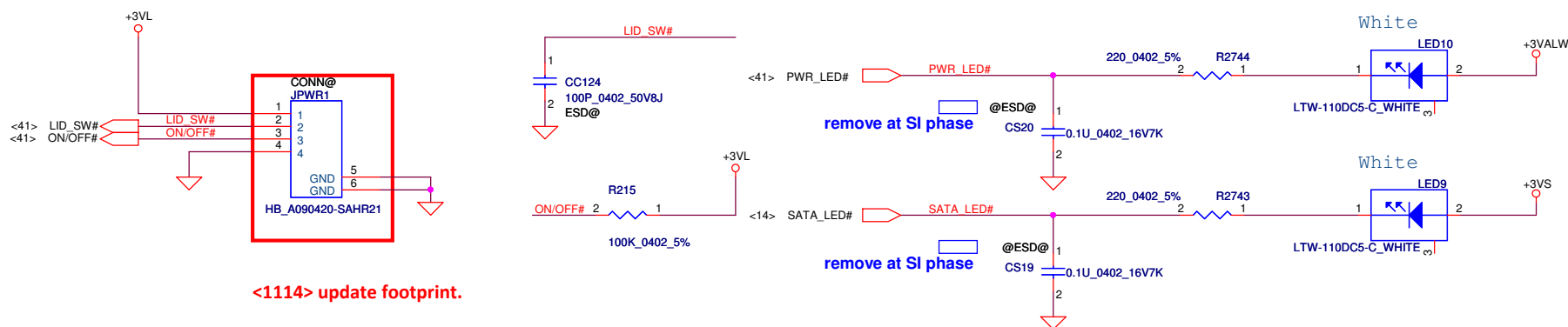


Keyboard conn

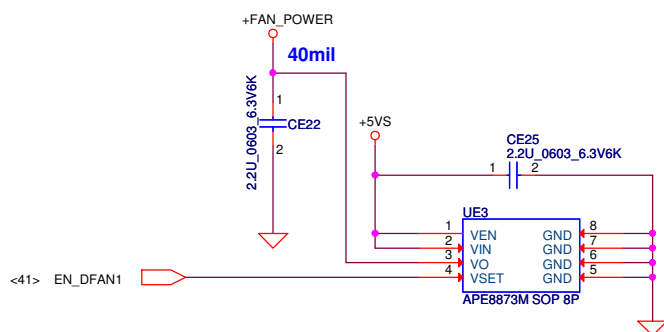


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				Date:	Thursday, February 20, 2014
		Sheet		38	of 58
		Rev		0.1	

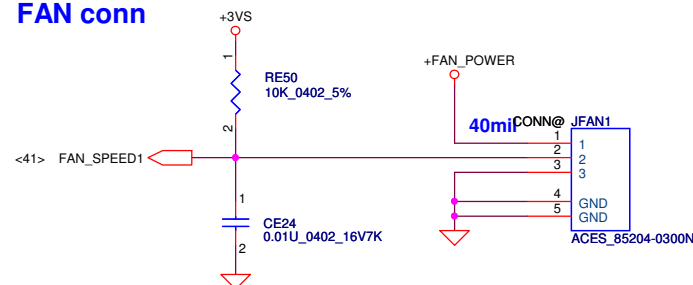
Power Button Connector



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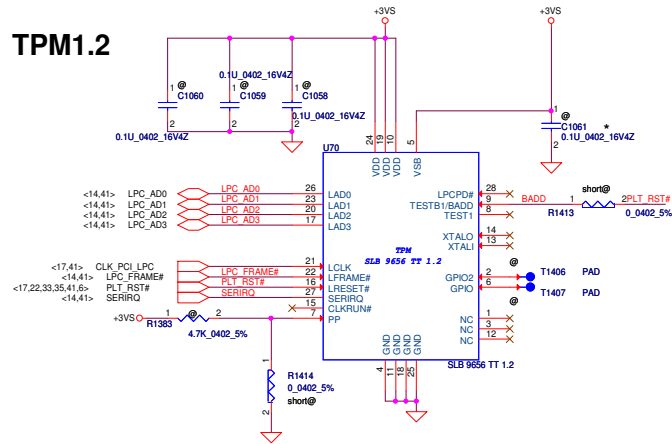


FAN conn

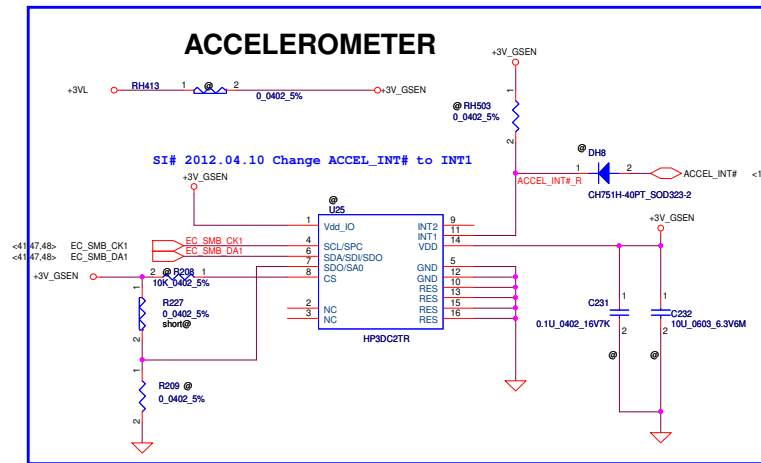


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				Date:	Thursday, February 20, 2014
				Sheet	39 of 58

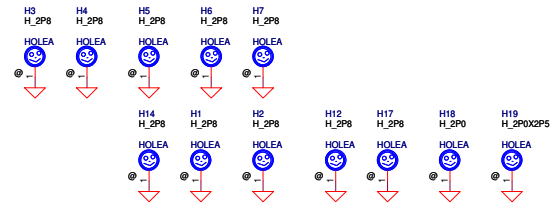
TPM1.2



ACCELEROMETER



Screw Hole

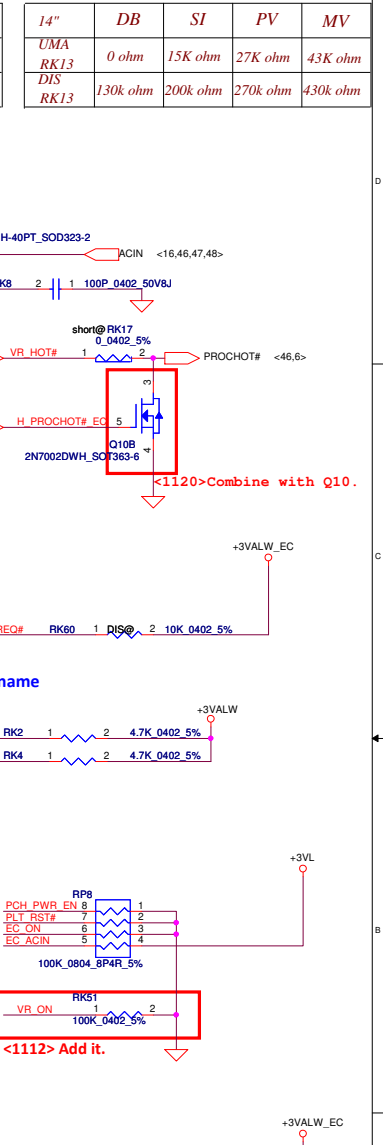
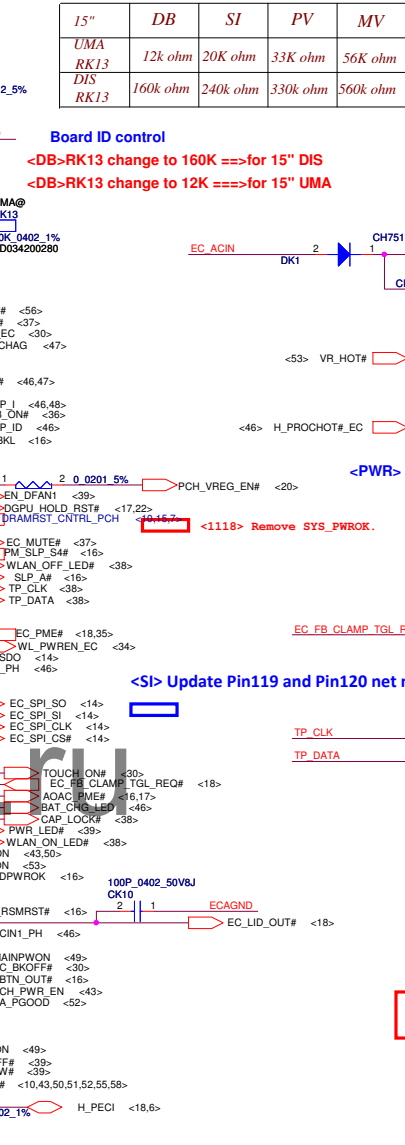
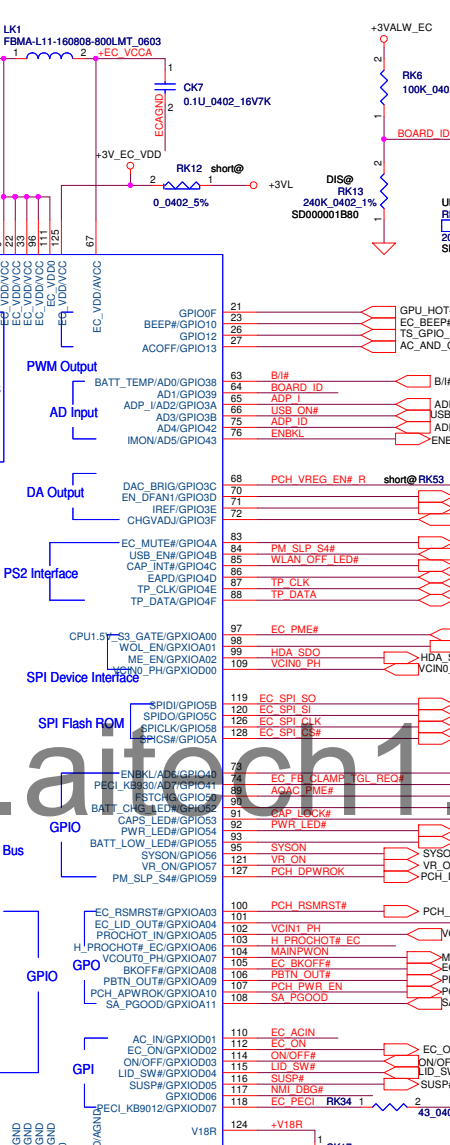
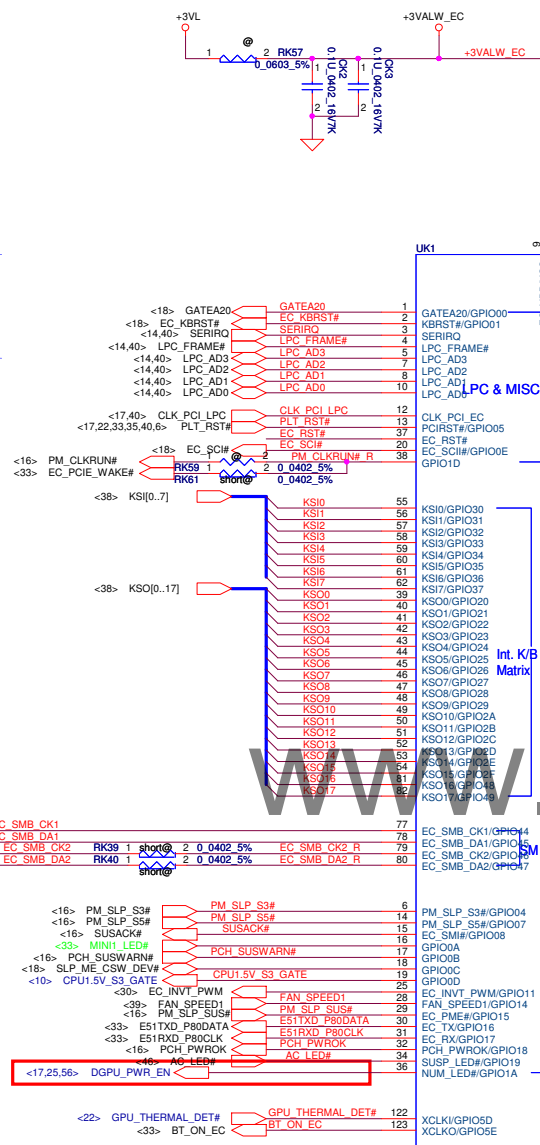
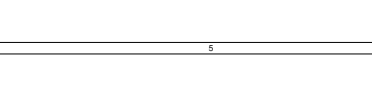
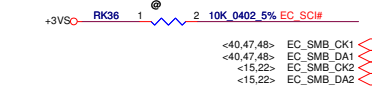
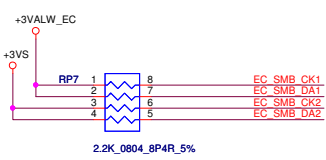
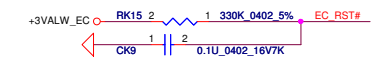
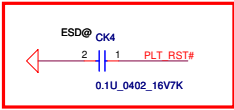


DAX
PCB
DA600016700

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Date: Thursday, February 20, 2014				Sheet 40	of 58

PV# 2013.01.29 Add CK4 for ESD protection



15"	DB	SI	PV	MV
UMA	12k ohm	20K ohm	33K ohm	56K ohm
RK13	12k ohm	20K ohm	33K ohm	56K ohm
DIS	160k ohm	240k ohm	330k ohm	560k ohm
RK13	160k ohm	240k ohm	330k ohm	560k ohm

14"	DB	SI	PV	MV
UMA	0 ohm	15K ohm	27K ohm	43K ohm
RK13	0 ohm	15K ohm	27K ohm	43K ohm
DIS	130k ohm	200k ohm	270k ohm	430k ohm
RK13	130k ohm	200k ohm	270k ohm	430k ohm

Board ID control

<DB>RK13 change to 160K ==>for 15" DIS
<DB>RK13 change to 12K ==>for 15" UMA

<1118> Remove SYS_PWROK.

<SI> Update Pin119 and Pin120 net name

<1112> Add it.

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Green CLK no reserved.
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BOM control

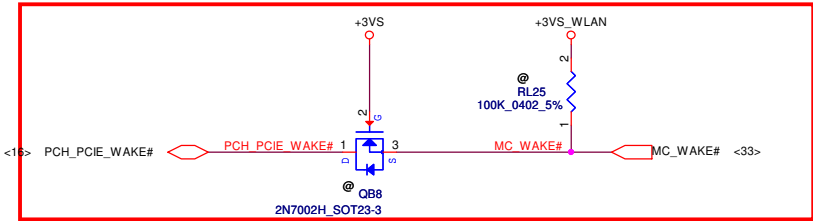
Platform	Silego P/N	Compal PN	25MHz(A)	32.768KHz	25MHz(B)	27MHz	8MHz	Remark
Intel CRV UMA	SLG3NB244VTR	SA000063300	1	1	1	X	X	GCLKUMA@
Intel CRV Dis	SLG3NB304VTR	SA000057100	1	1	1	1	X	GCLKDIS@

Base on A32 32.768KHz use 10ppm, G-CLK 25MHz X'TAL use 10ppm.

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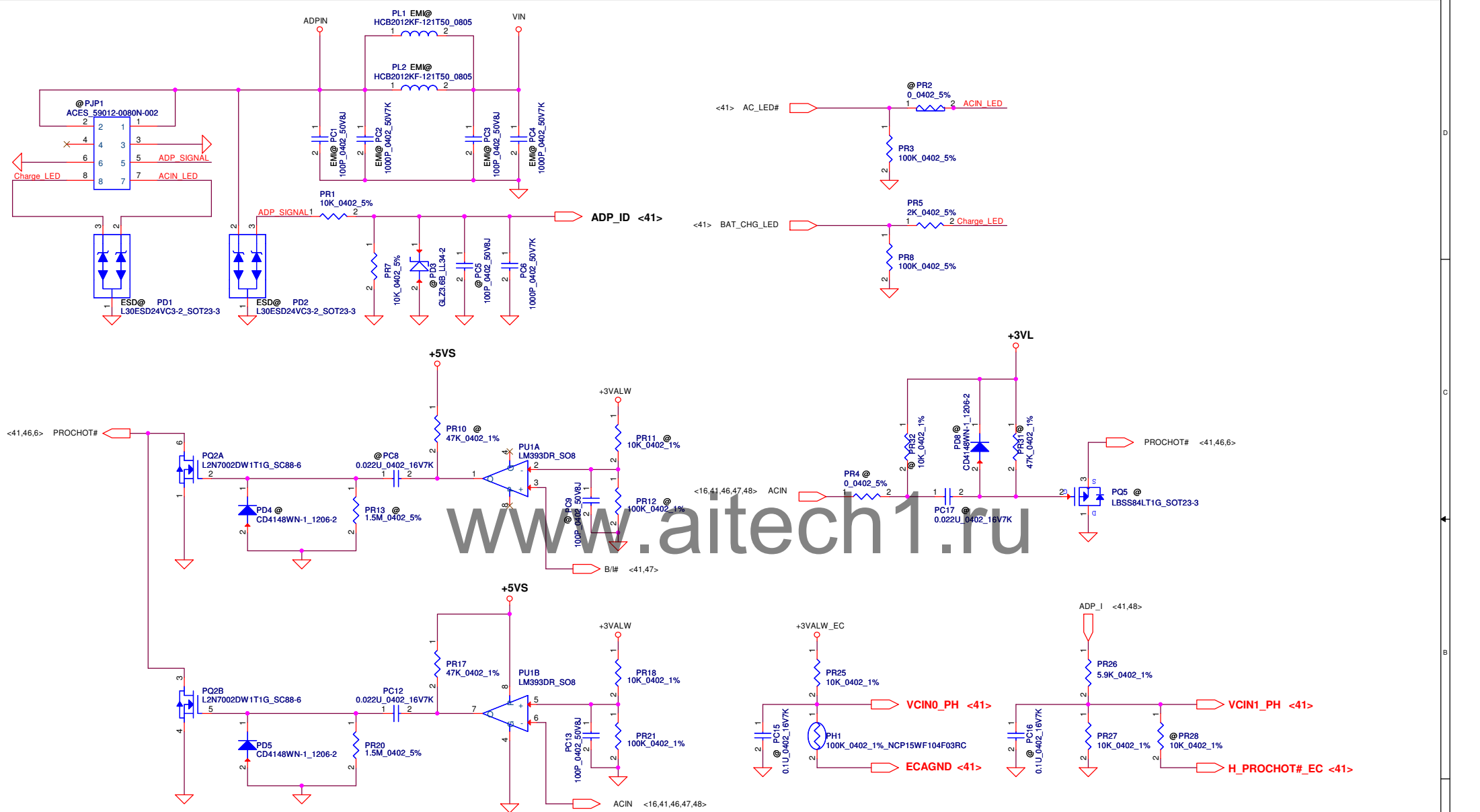
NGFF and WLAN



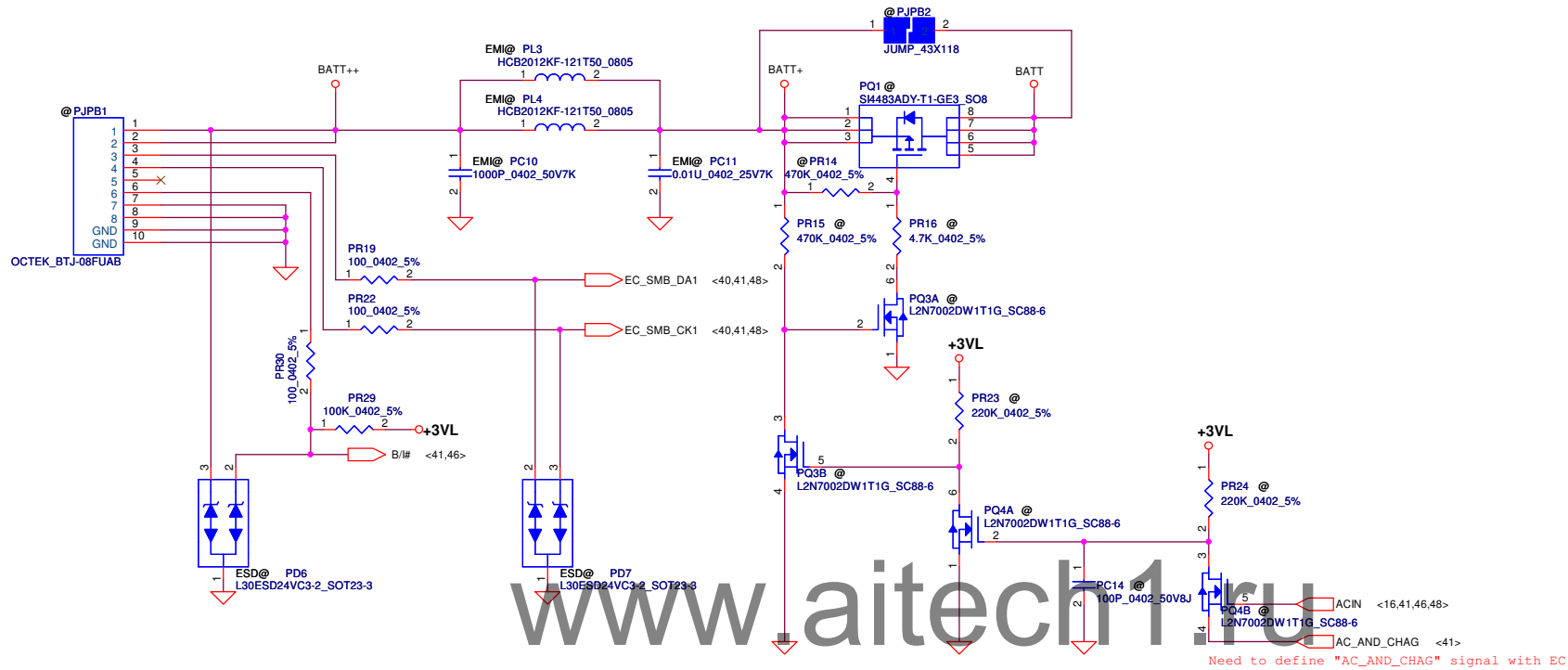
PV# 2013.01.23 Add QB8 abd RL25 to support OBFF
PV# 2013.02.22 Unpop QB4 and RL23 for not support OBFF

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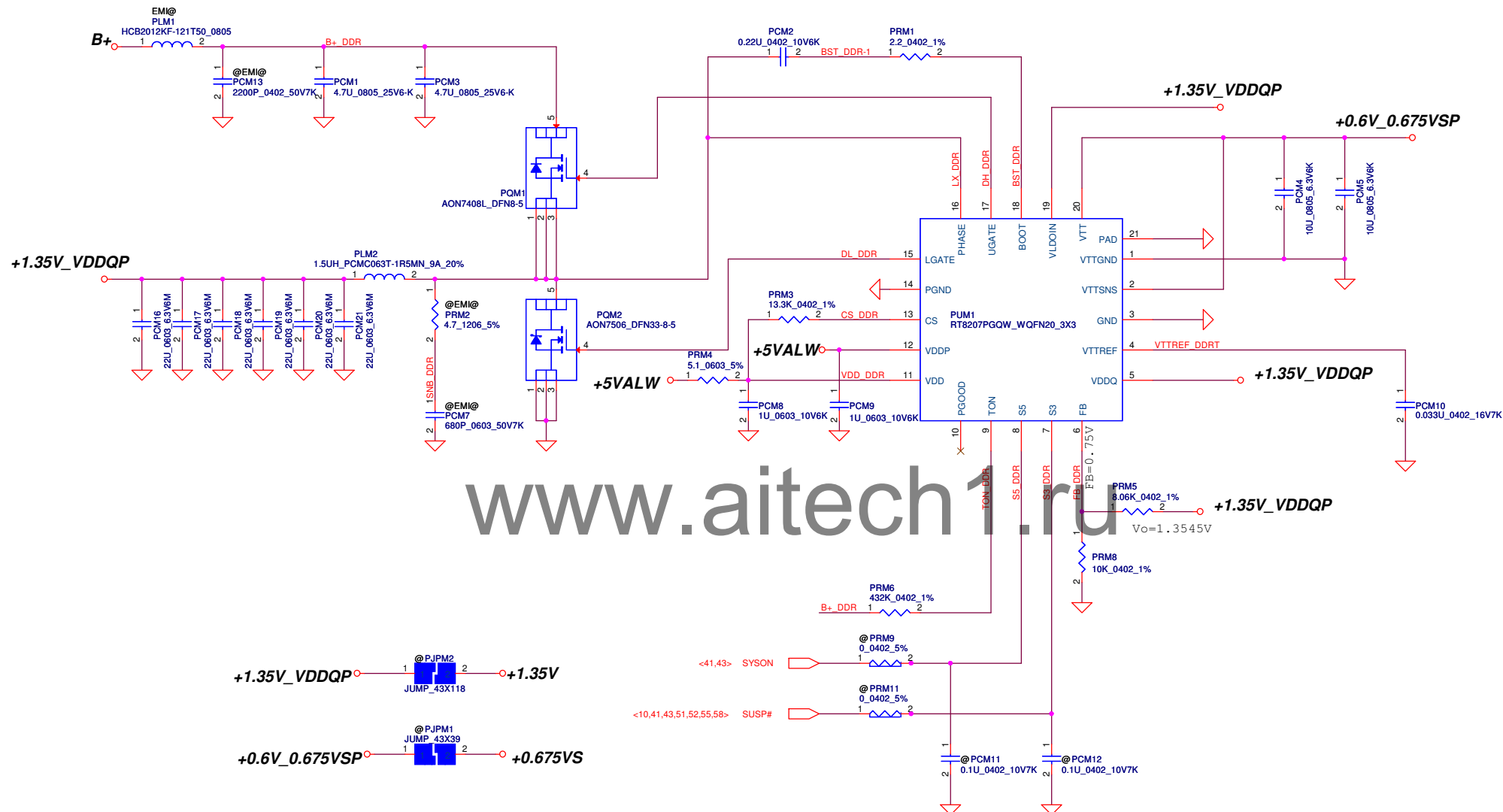
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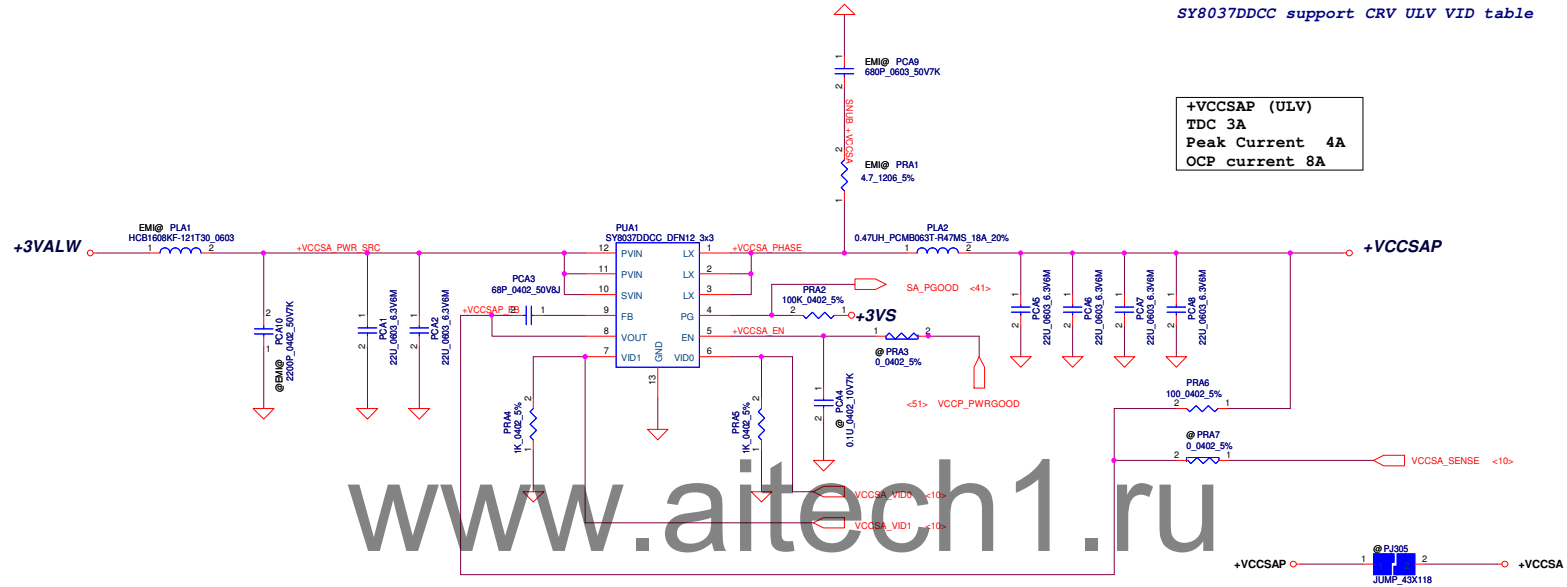


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VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

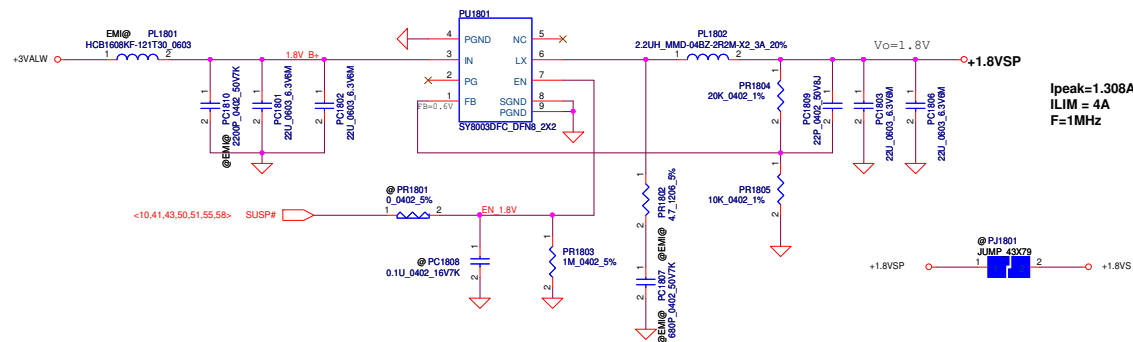
SY8037DDCC support CRV ULV VID table

+VCCSAP (ULV)
TDC 3A
Peak Current 4A
OCP current 8A



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The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.



Ipeak=1.308A
ILIM = 4A
F=1MHz

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Design Note
This circuit is for ULV i+1 17W.
CPU: IccMax=33A, TDC=16A(TDP NOM)
Loadline: -2.9 m V/A
Output Cap. follow Intel PDDG
330uF/9m*1, 560uF/4.5m*1 22uF_0603*12, 2.2uF_0402*16
GFX(GT2): IccMax=33A, TDC=21.5A
Loadline: -3.9 m V/A
Output Cap. follow Intel PDDG
560uF/4.5m*1, 22uF_0603*6, 10uF_0603*6, 1uF_0402*11

Close GFX choke

Close GFX L/S MOS

Close CPU L/S MOS

PRZ15 and PRG5
27.4K ohm for 100 degree
61.9K ohm for 110 degree

Layout Note
SVID routing
1. Alert# signal must be routed between the Clock and Date lines to reduce the cross talk between them. Signal order arrangement: mobile order is Clock-Alert-Date.
2. SVID spacing requirement is 18mils(0.475mm): VSSENSE
3. Maximum total microstrip routing length of each SVID signal must not exceed 6000mils(152.4mm).
4. The SVID bus must be ground reference. It cannot be referenced to input (Vbat or 12V) power plans as they can couple noise into the SVID bus as power states change.
5. Avoid routing under noisy circuit, e.g. switch node, Gate driver, B+, Vin, high speed signal.
6. When SVID signal changes Layer, GND return path may be changed also. We need add GND via for GND reference.

$C_n = L / ((R_{ntcnet} * R_{sum}) / (R_{ntcnet} + R_{sum})) * DCR$
If C_n is correctly selected, when the load current has a square change, the output voltage also has a square response.

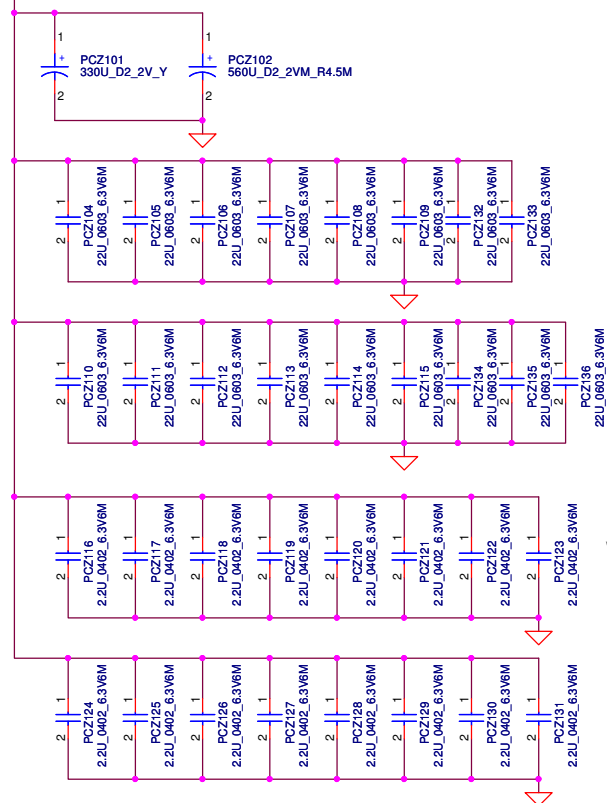
Layout Note
Reduce Acoustic Noise
1. The AL bulk capacitor of B+ should be very close to CPU_CORE MOSFET.
2. Input ceramic caps must place on symmetry same location on top side and bottom side.

OCP setting=39.9~44.99A

OCP setting=39.9~44.99A

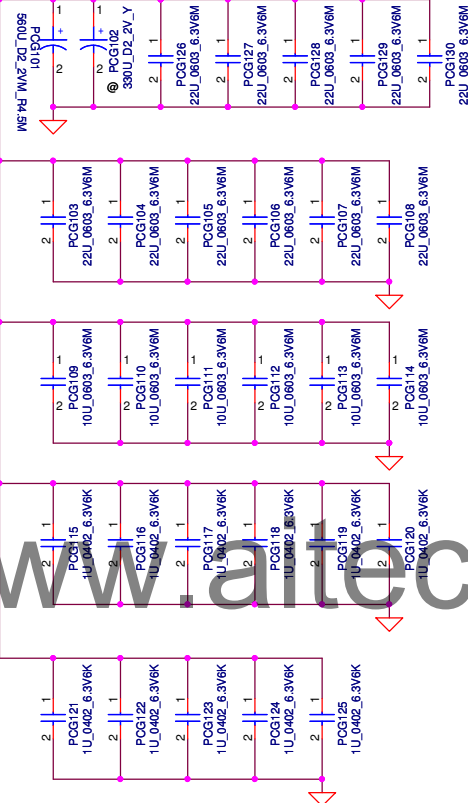
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+CPU_CORE



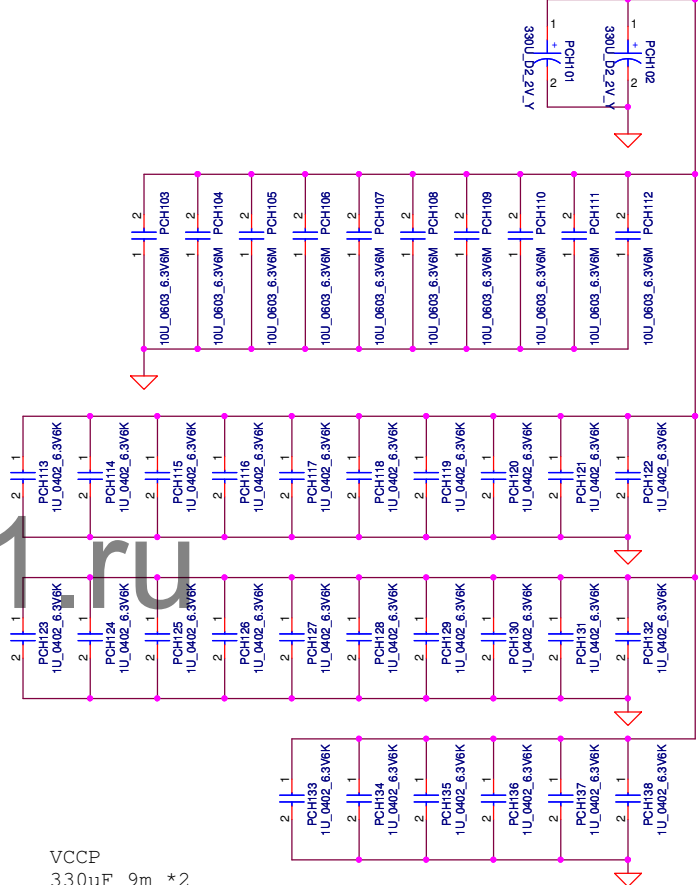
CPU_CORE
330uF 9m *1
560uF 4.5m *1
22uF 0603 *12
2.2uF 0402 *16

+VGFX_CORE



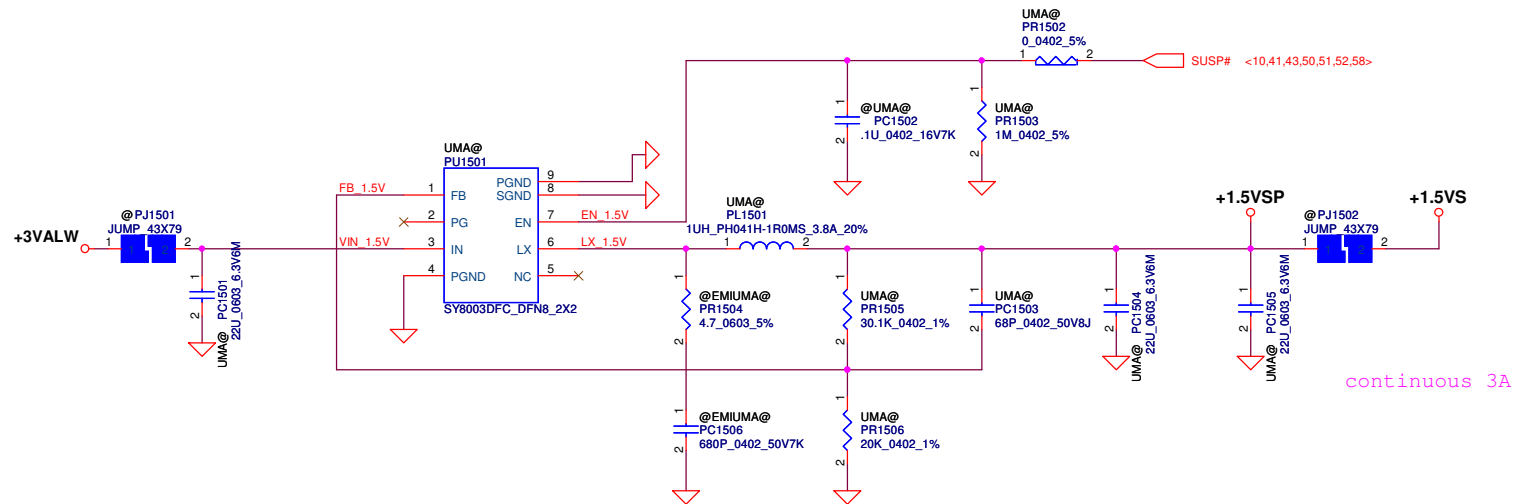
VGFX_CORE
560uF 4.5m *1
22uF 0603 *6
10uF 0603 *6
1uF 0402 *11

+VCCP



VCCP
330uF 9m *2
10uF 0603 *10
1uF 0402 *26

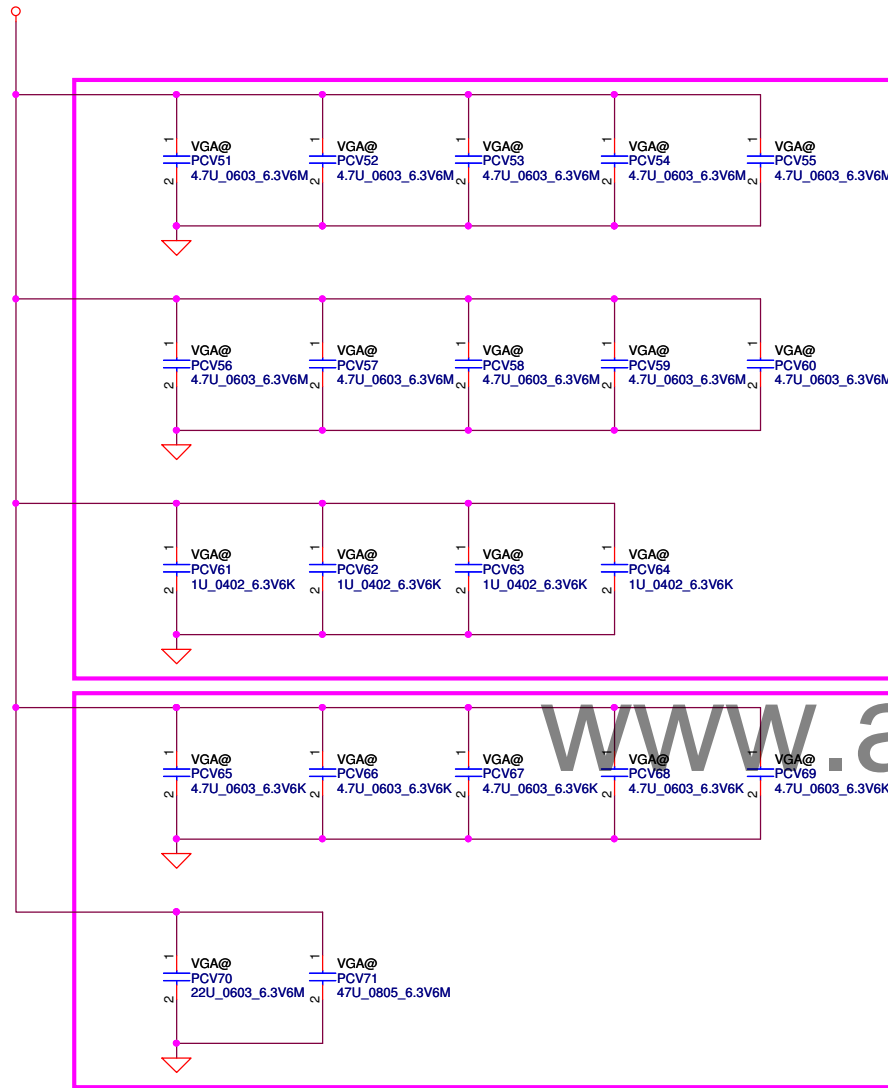
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+VGA_CORE



PLACE UNDER GPU

PLACE NEAR GPU

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